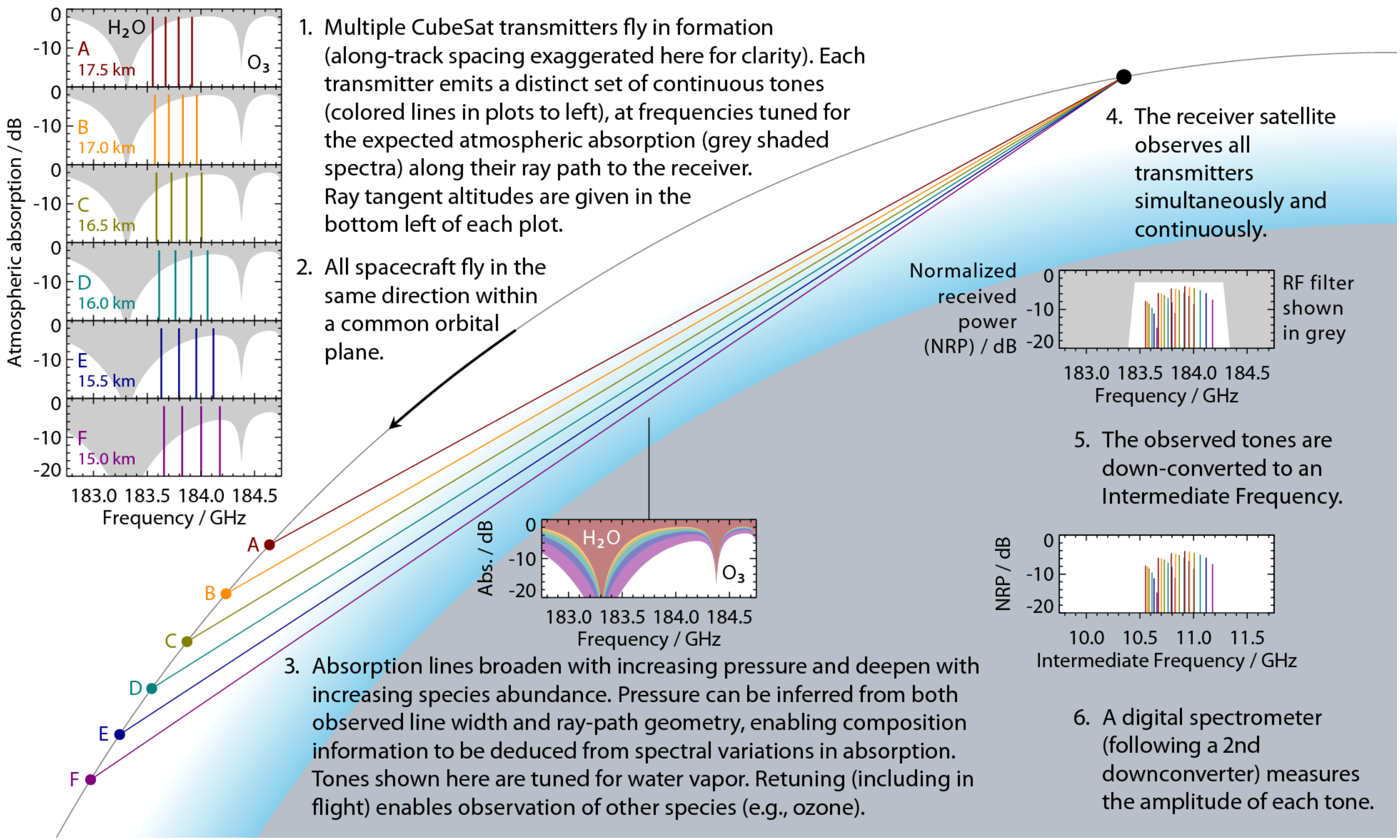
CMOS System-on-Chip Synthesizer development for the *"Stratospheric Water Inventory, Tomography of Convective Hydration"* (SWITCH) Instrument

(IIP-216)

<u>Adrian Tang</u>
University of California at Los Angeles

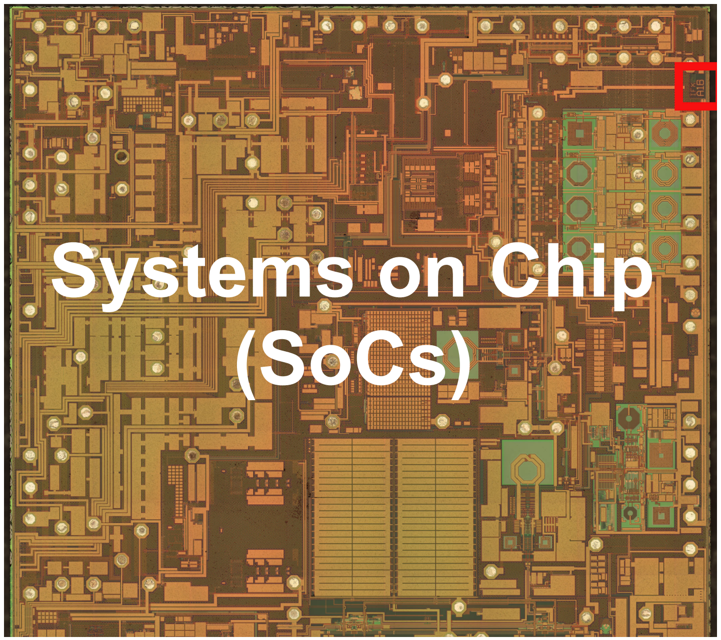
Nathaniel Livesey, Goutam Chattopadhyay, Theodore Reck, Robert Jarnot, Carl Felten, Jacob Kooi, Robert Stachnik, William Read, Adrian Tang
Jet Propulsion Laboratory,
California Institute of Technology

The SWITCH measurement concept



CMOS System on Chip Technology

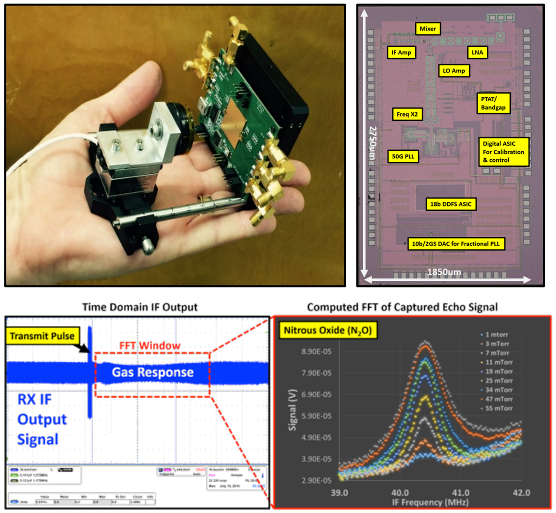
- The incredible integration ability of CMOS SoC technology is what enables modern electronics technology through reduction of system size/power.
- The ability to integrate 1000s of functions and sub-systems (analog, digital, mixed-sig, RF) onto a single-chip is what drives these industries.



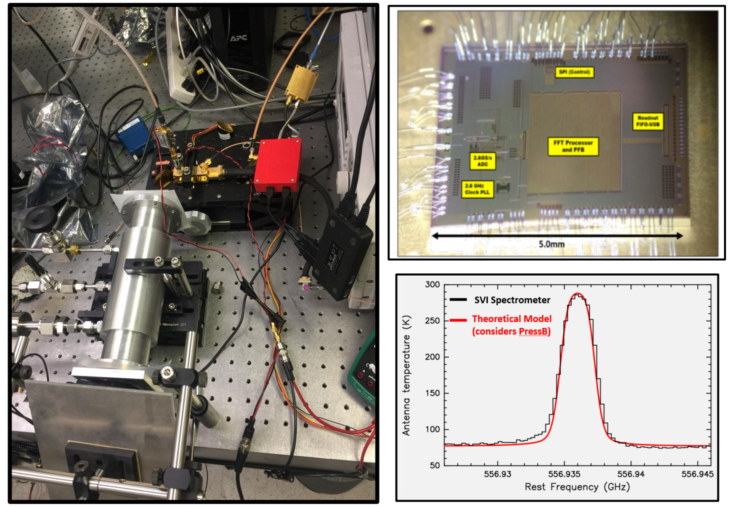
- **Can we use SoC technology to reduce size/weight and power of space instruments?**

Recent Demonstrations by the JPL-UCLA SoC Team

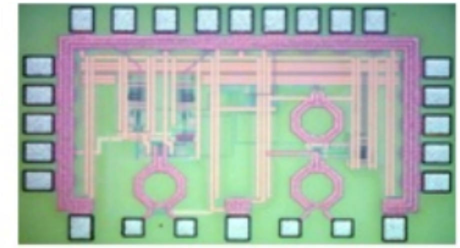
SoC Cavity Spectrometer
(tsmc 65nm gp-plus)



4k/6GS SoC Spectrometer Processor
(Developed in tsmc 28nm HPC)



60 GHz Transceiver



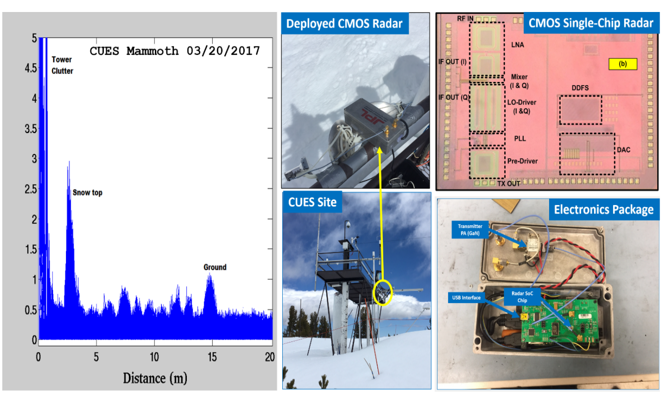
keyssa®

UCLA Spin-off Keyssa's 60 GHz short range transceiver is currently deployed in all new ACER laptops since Nov 2016.

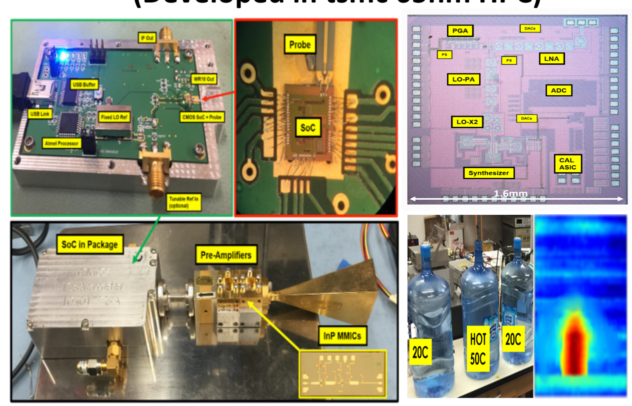
Currently shipping about 20M transceiver units a month including the SoC product and packaging solutions.

Market value at $52M
(www.keyssa.com)

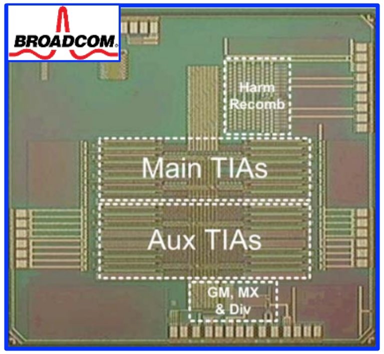
15 GHz SoC Radar
(tsmc 65nm gp-plus)



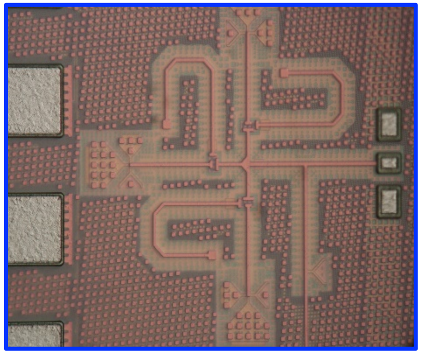
100 GHz SoC-InP Radiometer
(Developed in tsmc 65nm HPC)



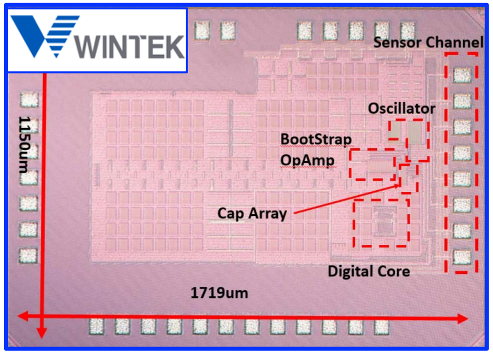
Major Achievements by UCLA's HSEL Laboratory



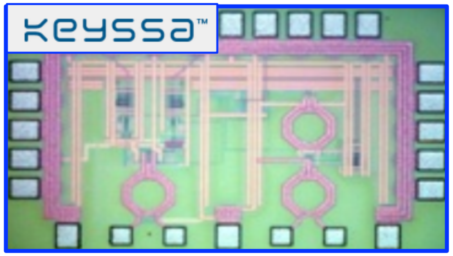
SDC gm-Cancelling Receivers
jointly developed by UCLA HSEL members David Murphy and Hao Wu with Broadcom. **Now used in almost every commercial 802.11 radio.**



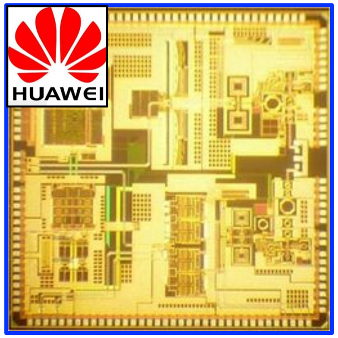
600 GHz Freq Synthesizer
World's fastest frequency synthesizer developed by HSEL members Yan Zhao and Richard Al Hadi, and Adrian Tang.



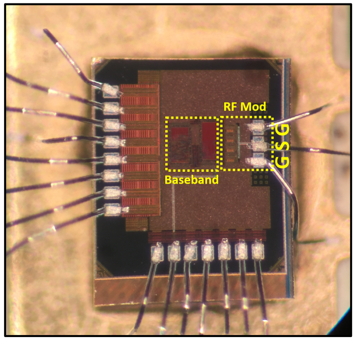
AirTouch Non-Contact Sensor
Extremely sensitive non-contact RF touch sensor developed for WinTek (Apple's touchscreen provider) by Li, Du, Yan Zhang, and Adrian Tang.



WaveConnect mmW Interconnect
Waveconnex (now Keyssa systems) mmW connector developed and commercialized by Rocco Tam and Rod Kim (now a JPL postdoc).

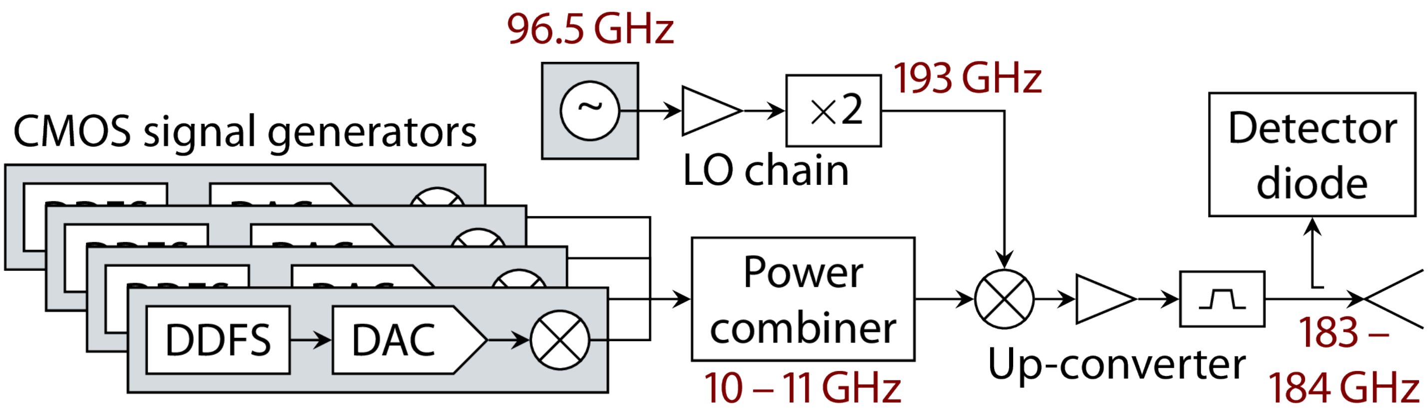


Full 802.11.ax 60G Transceiver
First demonstration of a full commercialized SoC supporting the 802.11.ax wireless standard. Developed by our entire team led by Adrian over last 2 years and currently being commercialized by Huawei in China.



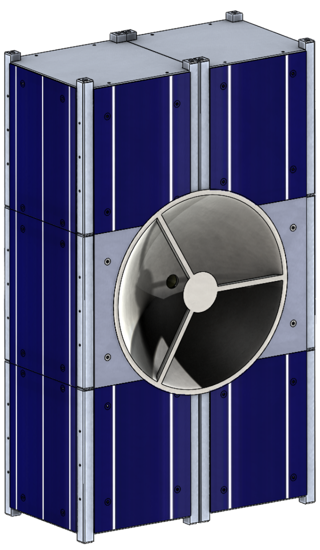
Reflector WiFi for Wearables
First demonstration of a fully compatible 802.11 reflector link for lower power In wearable devices. Developed by Adrian Tang.

SWITCH CubeSat transmitter



SWITCH transmitter system.
Grey boxes are ASIC/SoC chips.

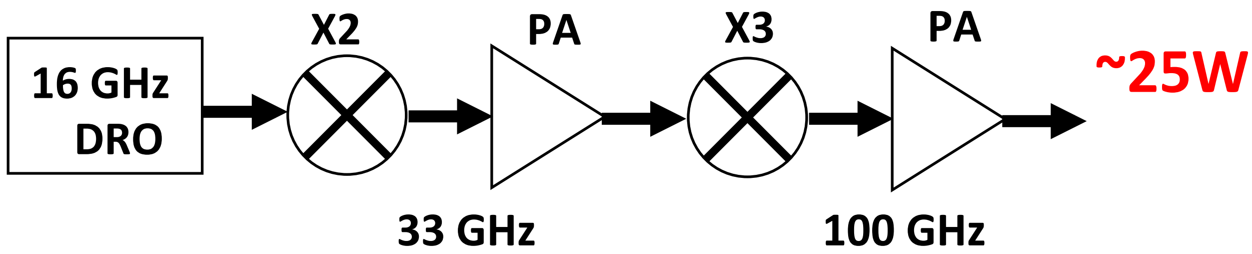
- SWITCH transmitters will be designed to be accommodated in 3U of a 6U CubeSat
- Key subsystems include:
  - Four CMOS 10–11 GHz programmable tone generators
  - A CMOS oscillator SoC providing a 96.5 GHz which is doubled to 193 GHz
  - An up-converter (GaAs Schottky mixer) and power amplifier (commercial component) boost these signals to 3 mW/tone
  - A conventional 15 cm Cassegrain reflector antenna



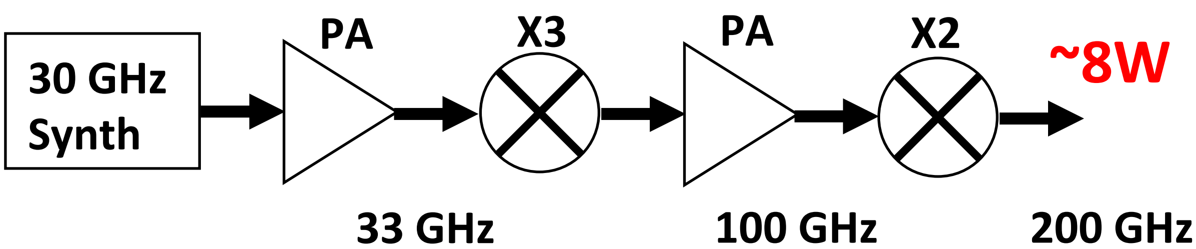
SWITCH transmit antenna integrated onto a 6U CubeSat

Advantage of Higher Frequency LO Synthesis

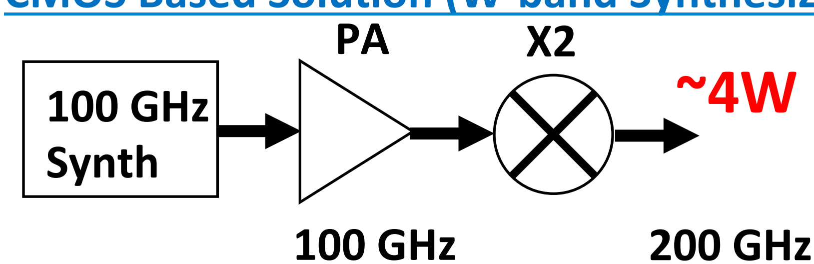
Pre-CMOS LO for a JPL 200 GHz Spectrometer (Before Adrian)



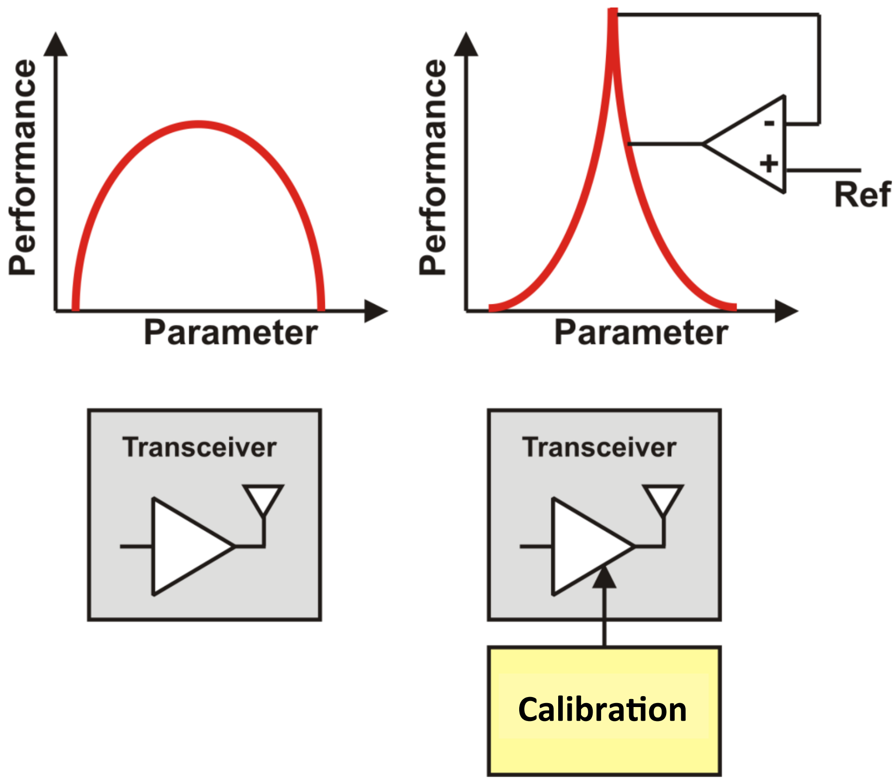
CMOS Based Solution (Ka-Band Synthesizer)



CMOS Based Solution (W-band Synthesizer)



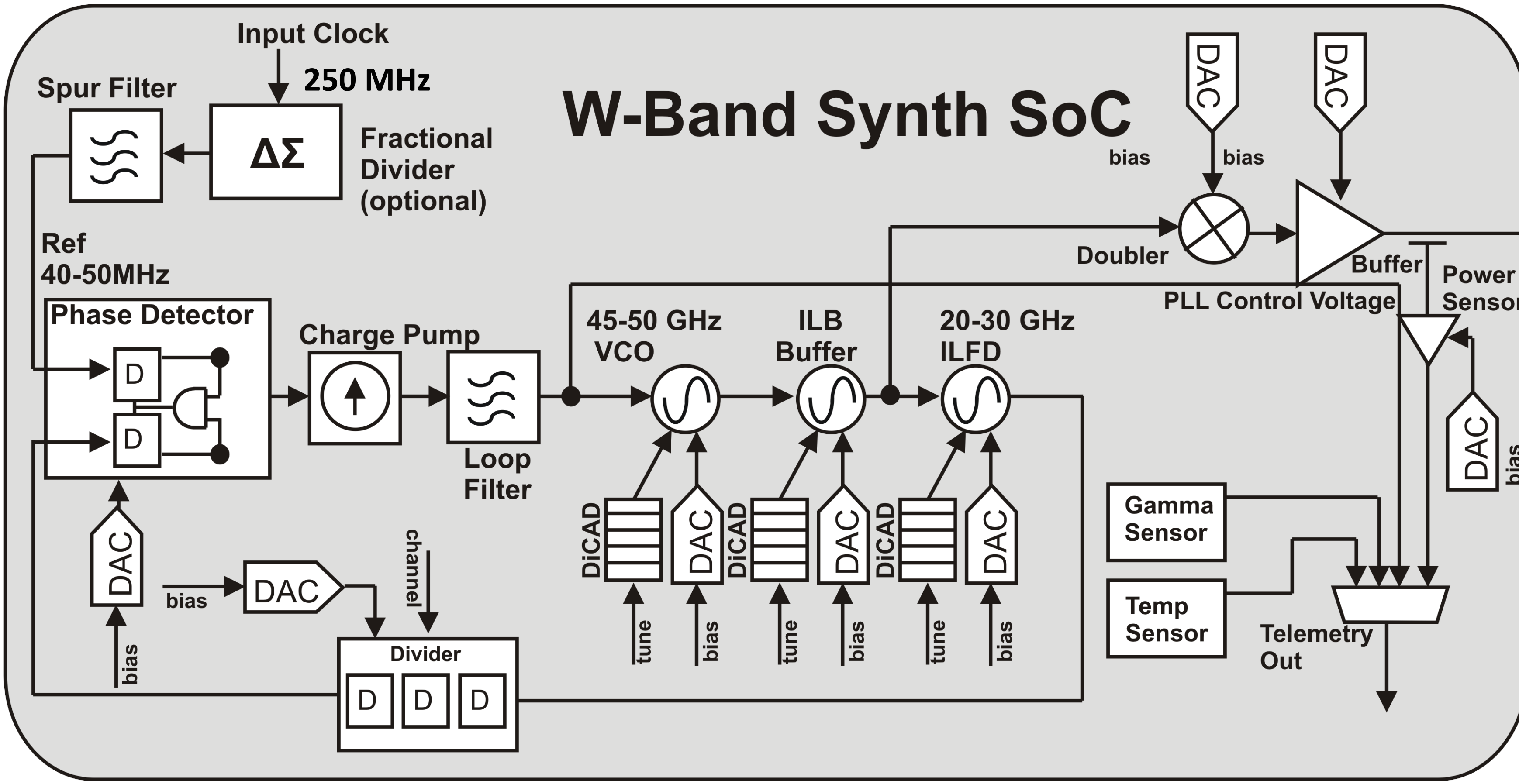
Modern High-Performance SoC Philosophy



- Modern SoCs are designed for tunability and flexibility, not peak performance or robustness!

- Modern SoC devices are not designed to be robust but instead integrate active and continuous calibration as part of their design.
- A continuous set of sensors and actuators continually monitors and adjusts performance of analog, mixed-signal and RF circuit parameters. (Background Calibration)
- Allows the design to be invariant to process and manufacturing variation at both the PCB and semiconductor levels.
- Also allows the device to be continually optimized for a changing environment (supply voltage, temperature, radiation)

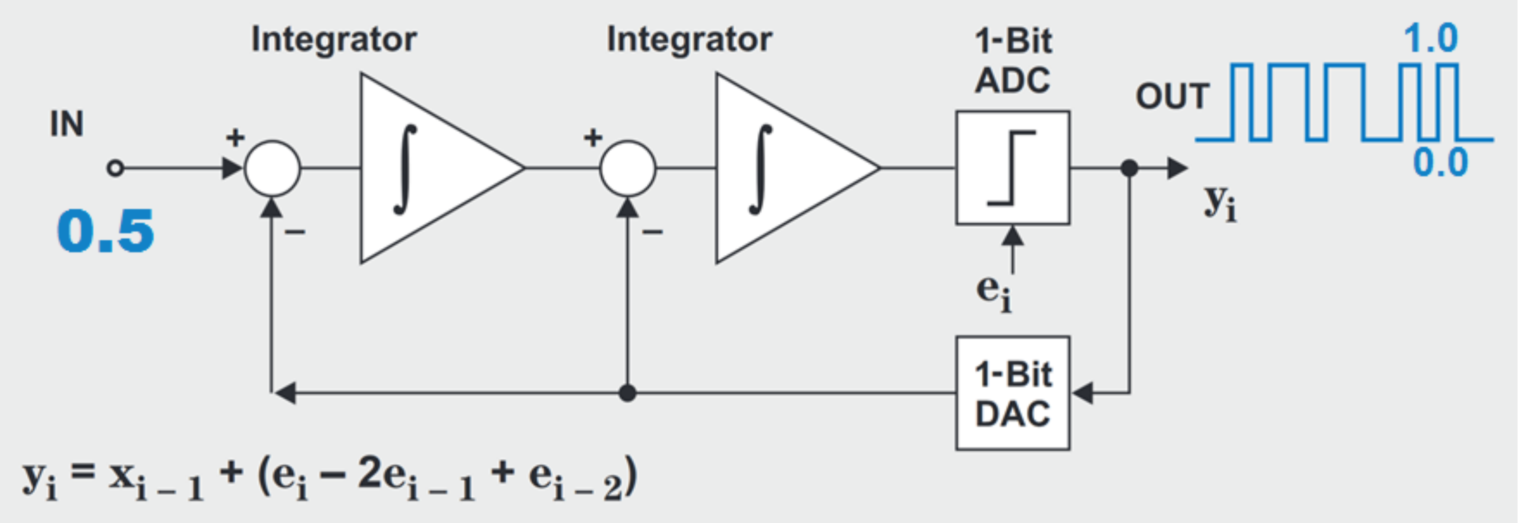
Block Diagram of Switch 89-102 GHz LO SoC



- Integrated frequency synthesizer, digital calibration (power, radiation, temp) sensors, and power amplifier into a single CMOS chip.
- Includes digital ASIC for RF power and phase-locked loop calibration.
- Compact and low power (226 mW) and only 2 x 2 mm^2 of die area in 65nm CMOS

ΔΣ - Fractional Frequency Synthesis

- Typically we need ~1 MHz LO tuning step size…. but typical clocks are 200-300 MHz which sets the minimum step size for integer-n PLLs. With multipliers this becomes even worse. The chip presented here as a 4 GHz step size in integer mode.
- Instead we rely on ΔΣ modulation to get fractional step sizes. A basic ΔΣ system switches between two states in a pseudo-random fashion so that the average frequency is a value between the two states.
- If we switched between states with a repeated sequence instead of with a random sequence we would create periodic content and spurs in the output of the synthesizer.

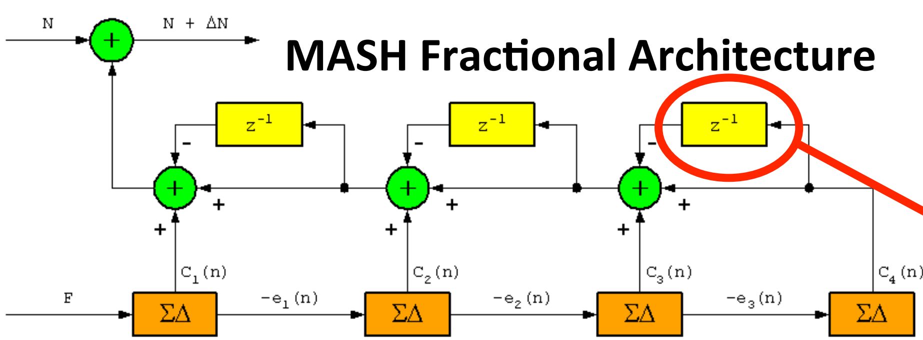


MASH ΔΣ for Fractional Synthesis

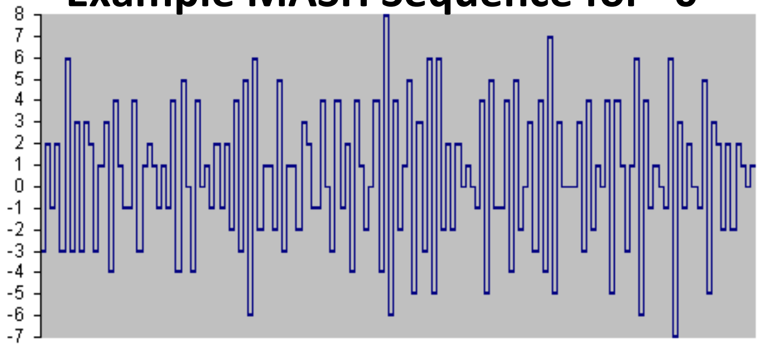
- Typically 2 levels is not high enough entropy or "random enough" to ensure no spurs so we adopt a multi-level architecture called Multi-stAge noise Shaping (MASH ΔΣ) that allows even more randomness and lower added spectral content.

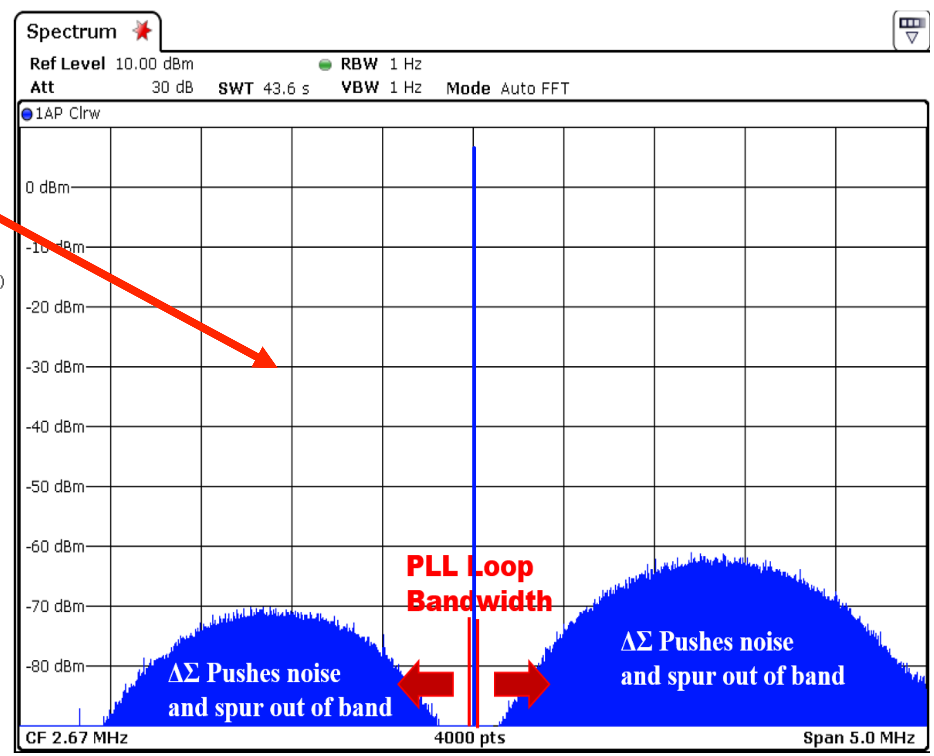
- A 4th order MASH (16 levels) used in the SWITCH LO design. Manipulation of the feedback coefficients allows remaining noise to be shaped out of the loop bandwidth.

MASH Fractional Architecture



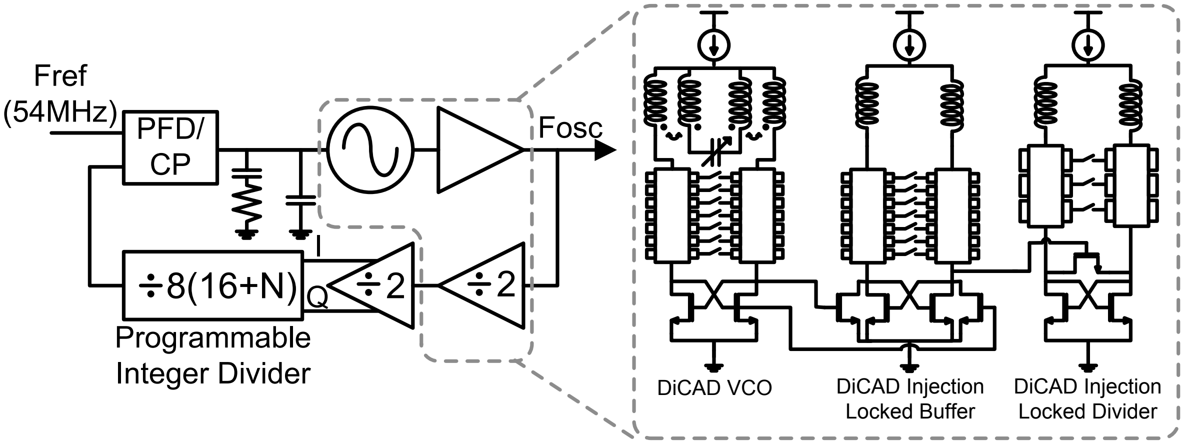
Example MASH Sequence for "0"



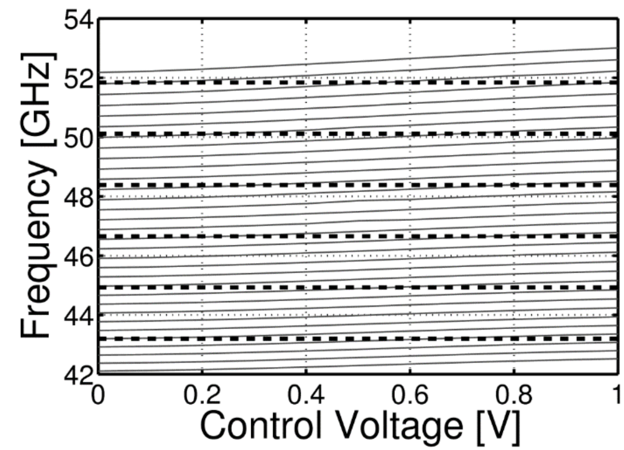


Core 40-50 GHz Synthesizer Design

Synthesizer Architecture



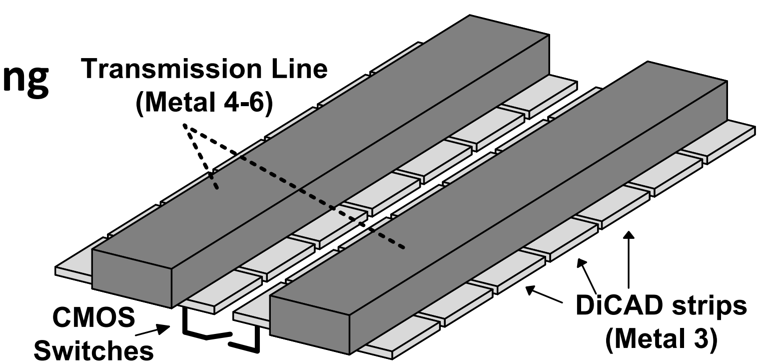
Open Loop Tuning



Core Frequency Synthesizer

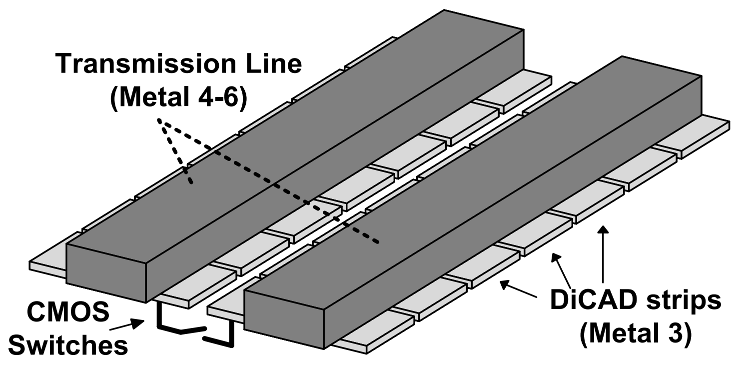
- Based on traditional injection locked division
- Digital Controller artificial dielectric (DiCAD) tuning
- Open loop coverage across the 40-50 GHz band
- Injection locked output buffer
- CML Static divider stages for high-speed

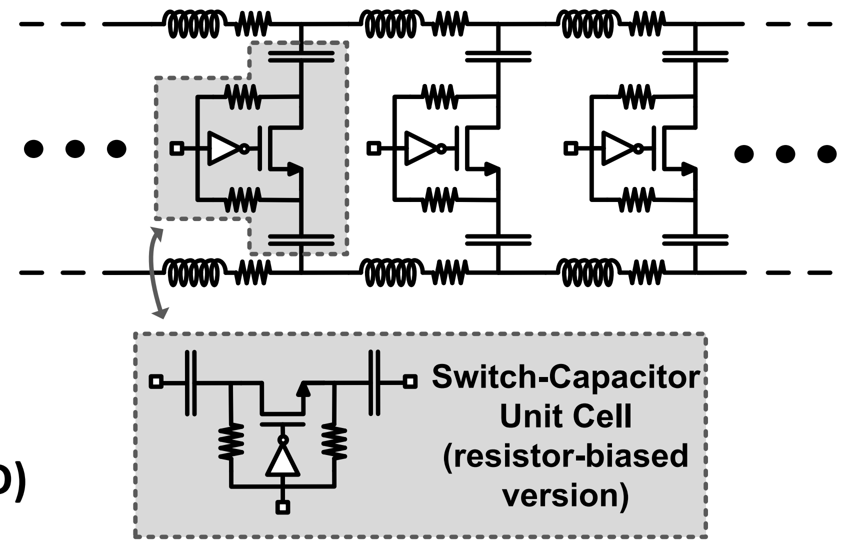
DiCAD Tuner



*A. Tang, D. Murphy, F. Hsiao, G. Virbila, Y.H. Wang, H. Wu, Y. Kim and M.F. Chang, "A CMOS D-Band Transmitter with IF Envelope Feed-Forward Pre-Distortion and Injection Locked Frequency Tripling Synthesizer" *IEEE Transactions Microwave Theory and Techniques* Vol 60, No 12, Dec 2012

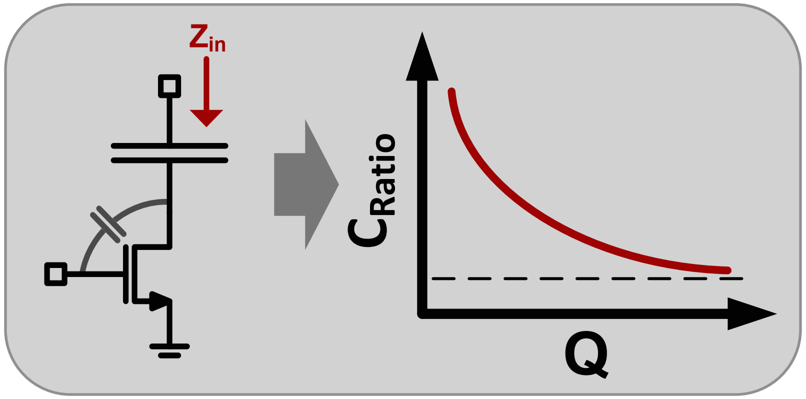
DiCAD Tuning Structure





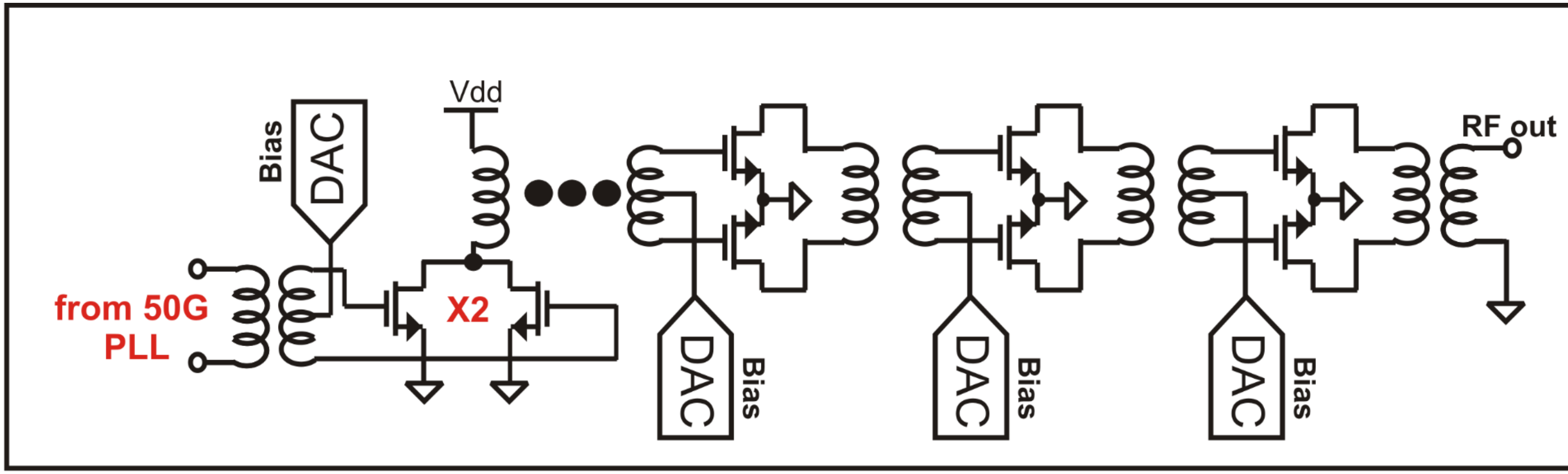
- ❖Digital Controlled Artificial Dielectric (DiCAD) is a digital tuning element which allows coarse band selection for mm-wave oscillators by adjusting TL permittivity.

- ❖Allows ILFDs and ILOs to partially shift their lock range left and right to achieve some overlap and further mitigate PVT variation.



*A. Tang, David Murphy, Gabriel Virbila, Frank Hsiao, Sai-Wang Tam, Hsing-Ting Yu, Yanghyo Kim, Alden Wong, Alex Wong, Yi-Cheng Wu, Mau-Chung Frank Chang, "D-Band Frequency Synthesis Using a U-band PLL and Frequency Tripler in 65nm CMOS Technology" IEEE International Microwave Symposium 2012.

RF Amplifier Chain Design



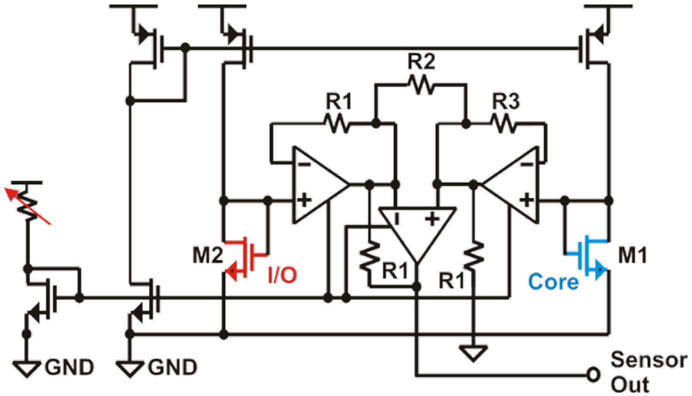
- 50-to-100 Frequency Doubler is a push-push architecture
- Regular CS-caterpillar amplifier chain with 5 stages
- All stages are DAC biased to allow for calibration and optimization
- Output stage bias is controlled as part of the auto-levelling loop.
- Power is monitored from output side of output transformer.

Measured TX Performance

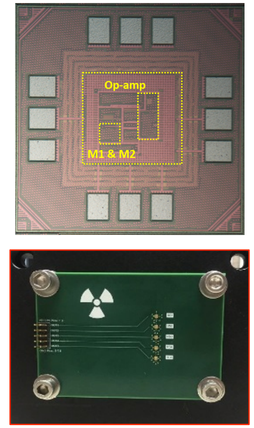
Parameter	Value
Output Power (Max)	6.0 dBm (4.0mW)
PA Bandwidth (3 dB)	87.1-105 GHz
“off-mode” Isolation	20 dB
Pulse Resolution	1 ns
Power Consumption	226 mW (inc. pll)

TID Radiation Sensor (Dosimeter) Design

Sensor Schematic

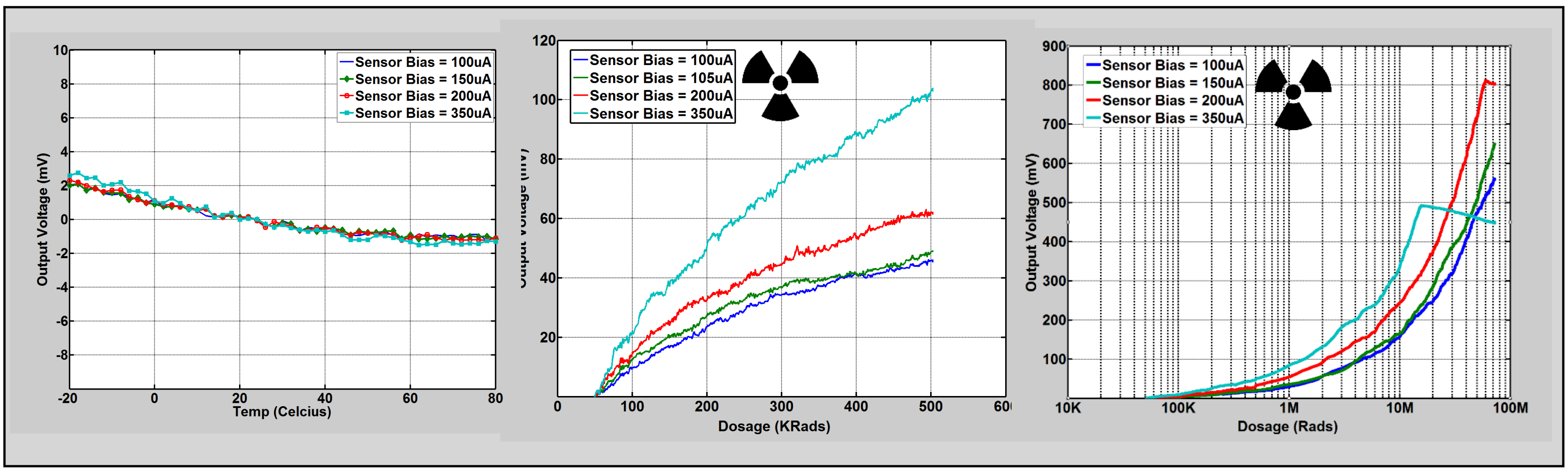


Test Chip



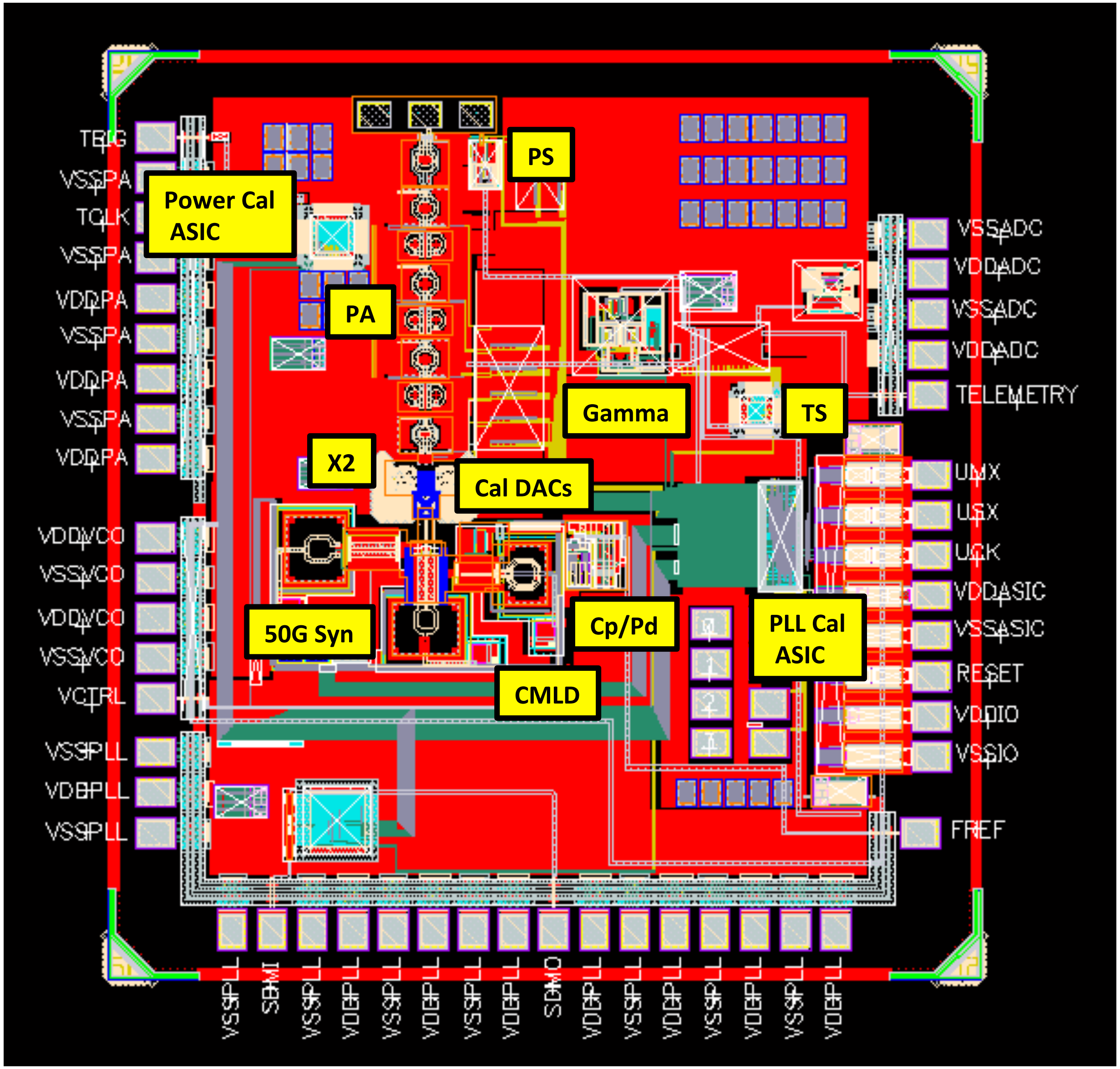
- Radiation monitoring is a serious issue for planetary missions.
- 65nm is relatively radiation insensitive so implementing a sensor the traditional way (radfet/fg) is difficult. The sensor also needs to be temperature insensitive .
- Developed a new radiation sensor that compares logic and I/O behavior to de-embed the temperature from radiation effects.

Radiation Sensor Performance

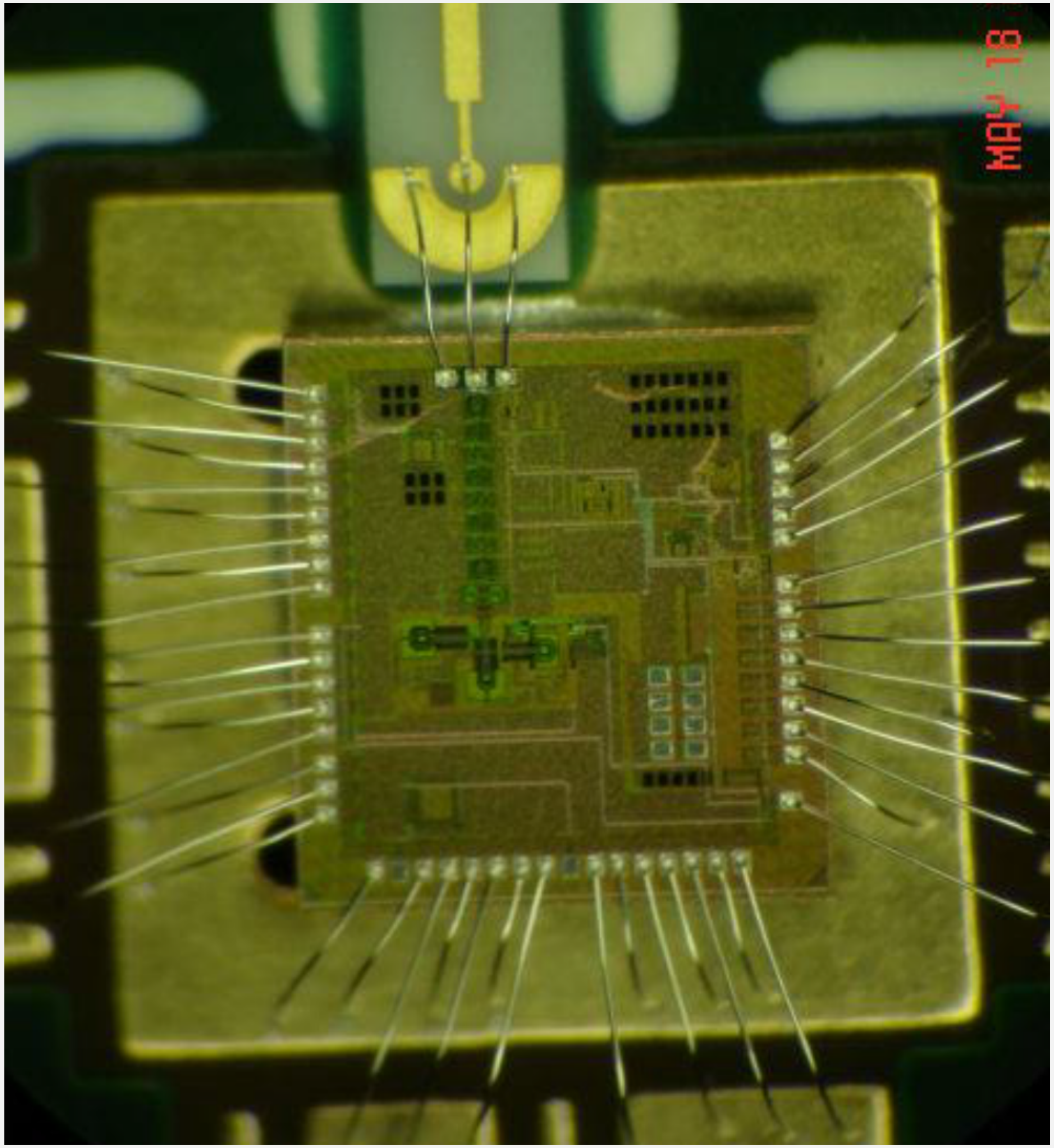


*A.Tang, Y. Kim, MC-Chang, "Logic-I/O Threshold Comparing Gamma Radiation Dosimeter in Insensitive Deep-Sub-Micron CMOS", *IEEE Transactions on Nuclear Science*, Vol 63, No. 2, Part 3, pp 1247-1250, April 2016.

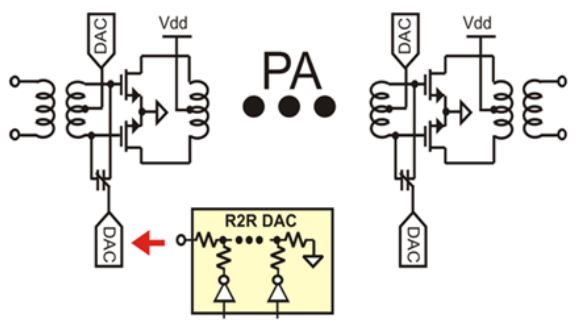
Top Level Layout and Die Photo

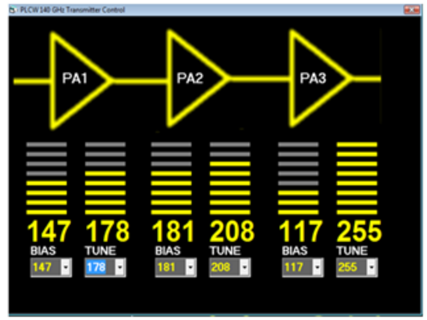


Top Level Layout and Die Photo

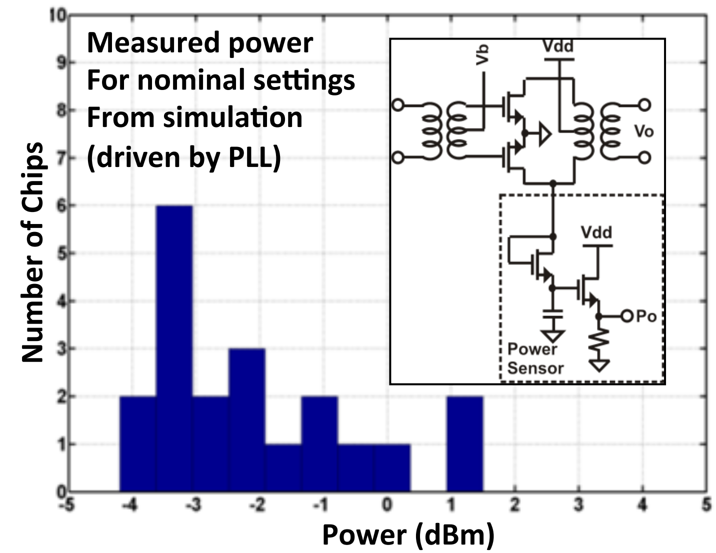


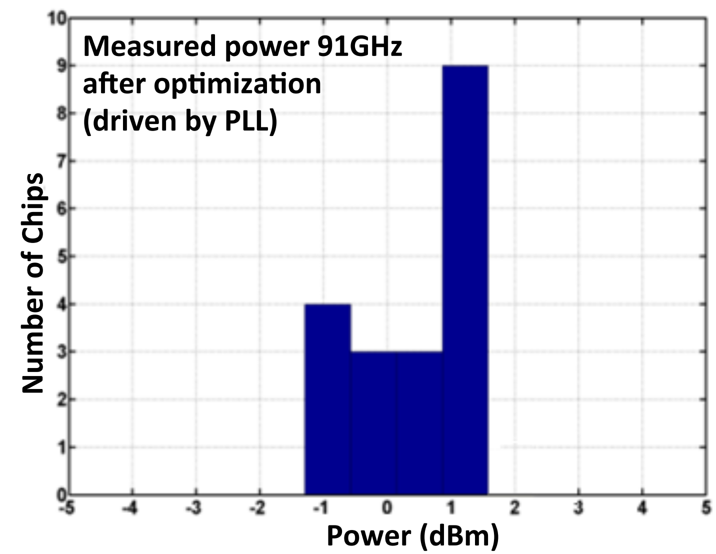
Internal Power Calibration System





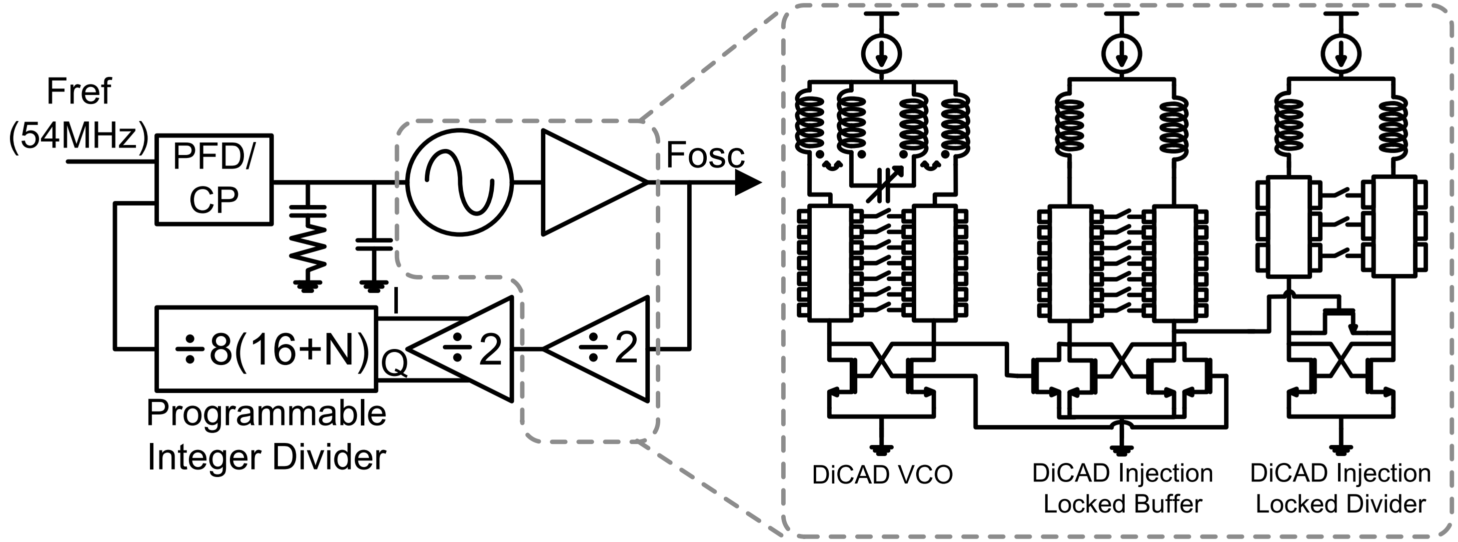
- ❖ Use DACs to adjust bias and varactor tuning to correct centre frequency and impedances.
- ❖ Output power is captured via a power sensor on each stage and fed to an ADC.
- ❖ Binary search algorithm is run on an internal ASIC processor to find optimal setting for output power.
- ❖ Demonstrates both a reduction of variation from chip-to-chip and an increase in the mean output power.





C. Chien, A. Tang, M.F. Chang, "Dual-Control Self-Healing Architecture for High-Performance Radio SoCs" IEEE Design and Test of Computers. September 2012.

Internal Phase-Lock Calibration

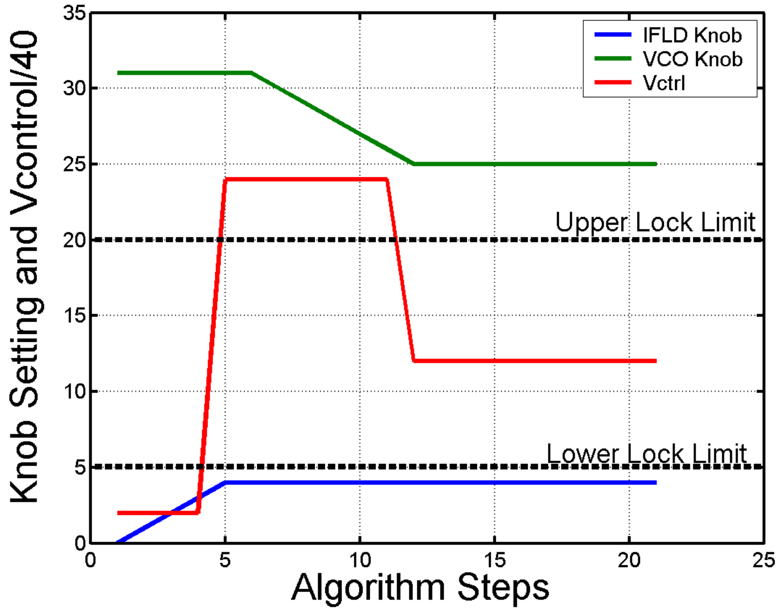


- **The DiCAD coarse tuning must be set with an algorithm on the ASIC so the lock ranges overlap and the PLL will lock:**
- **Sweep each stage from min-to-max starting closest to the Div and when a ctrl-V transition occurs move to the next stage.**
- **On the last stage keep tuning until the control voltage is between 20% and 80% of VDD by monitoring the window comparator.**
- **If the process fails try again except tuning max-to-min as lock ranges may not be symmetric around the free-running freq.**

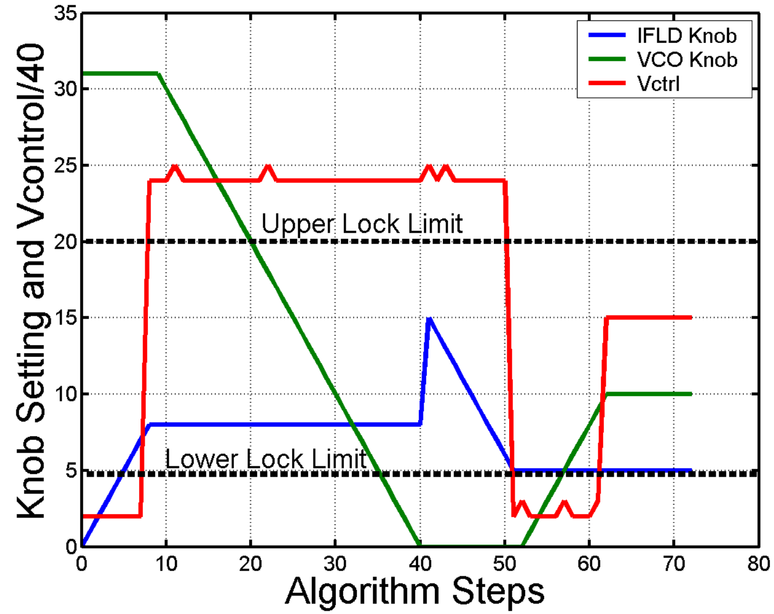
A. Tang, et-al., "A Low Overhead Self-Healing Embedded System for Ensuring High Performance Yield and Long-Term Sustainability of a 60GHz 4Gbps Radio-on-a-Chip" *IEEE International Solid-State Circuits Conference* 2012.

Internal Phase-Lock Calibration

Min to Max



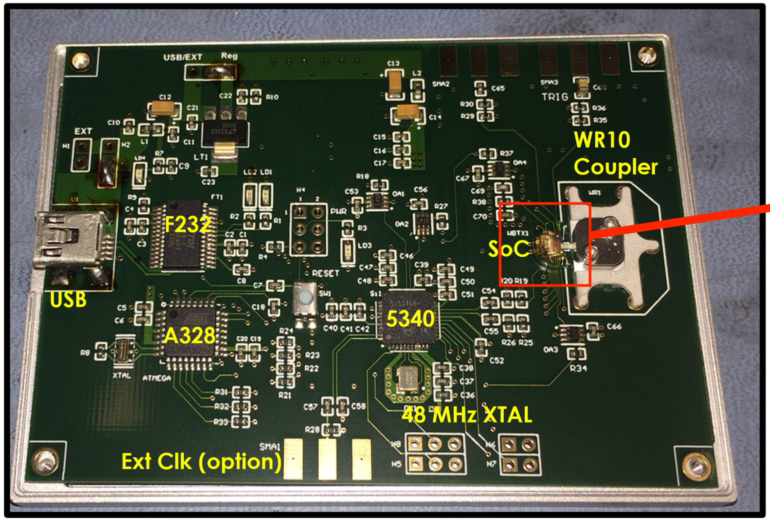
Max to Min

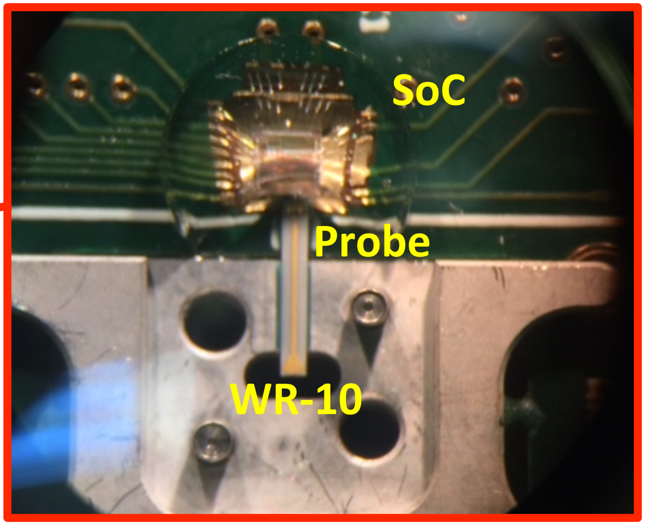


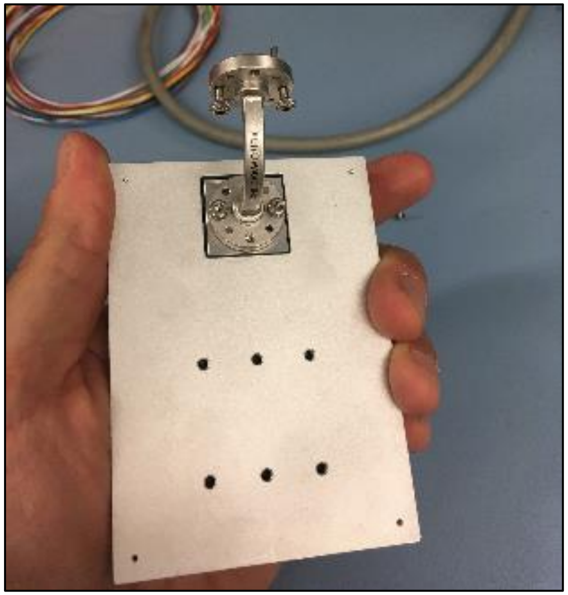
- ❖ **In a test of 20 chips, 15 locked in the (min to max) mode and 5 locked in the (max to min) mode. All chips locked.**
- ❖ **Algorithm will converge to suppress changes in supply voltage, radiation and temperature.**

*A. Tang, et-al., "A Low Overhead Self-Healing Embedded System for Ensuring High Performance Yield and Long-Term Sustainability of a 60GHz 4Gbps Radio-on-a-Chip" *IEEE International Solid-State Circuits Conference* 2012.

Synthesizer Packaging and Assembly

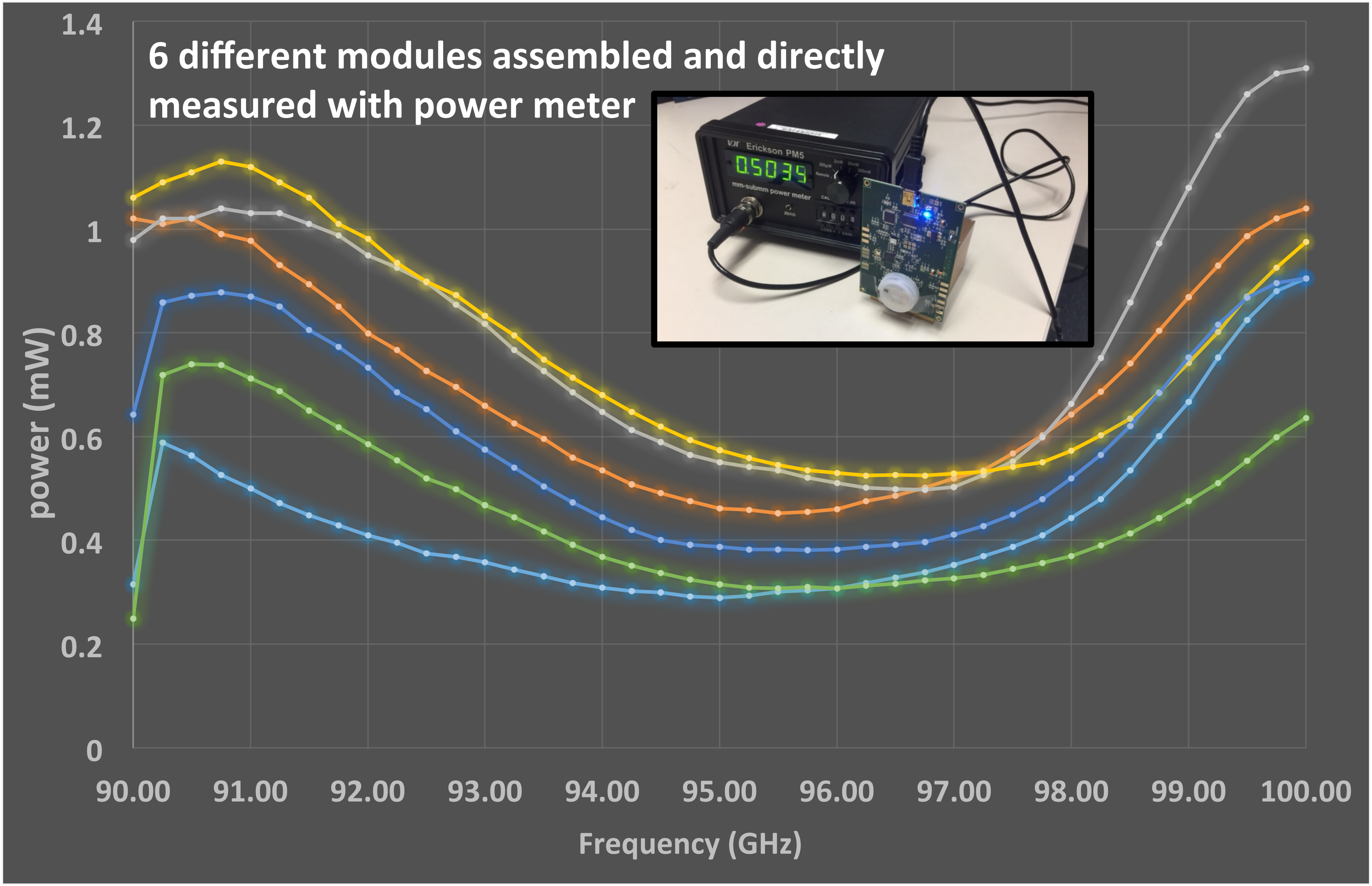




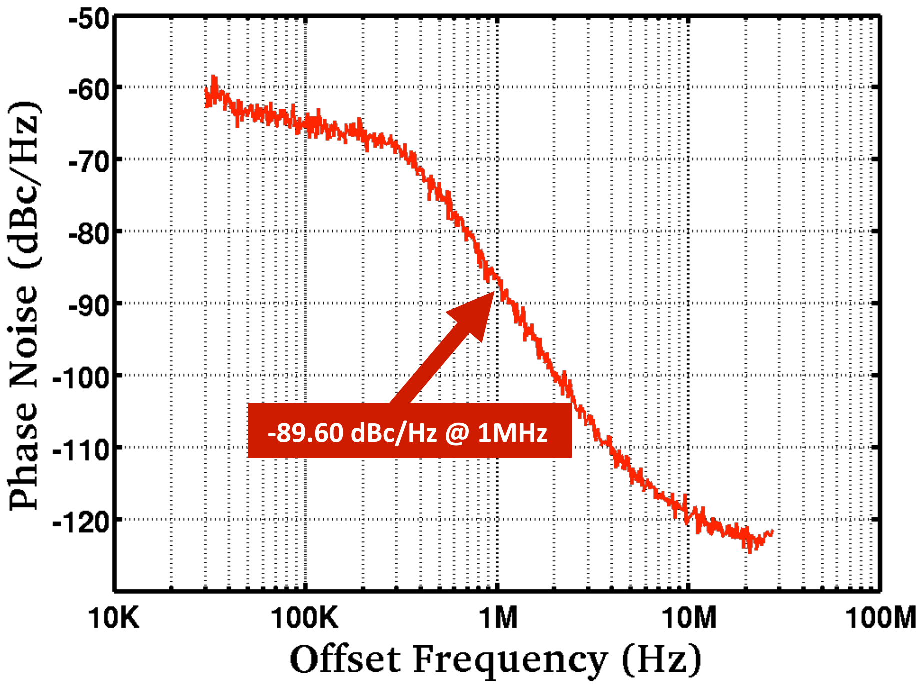


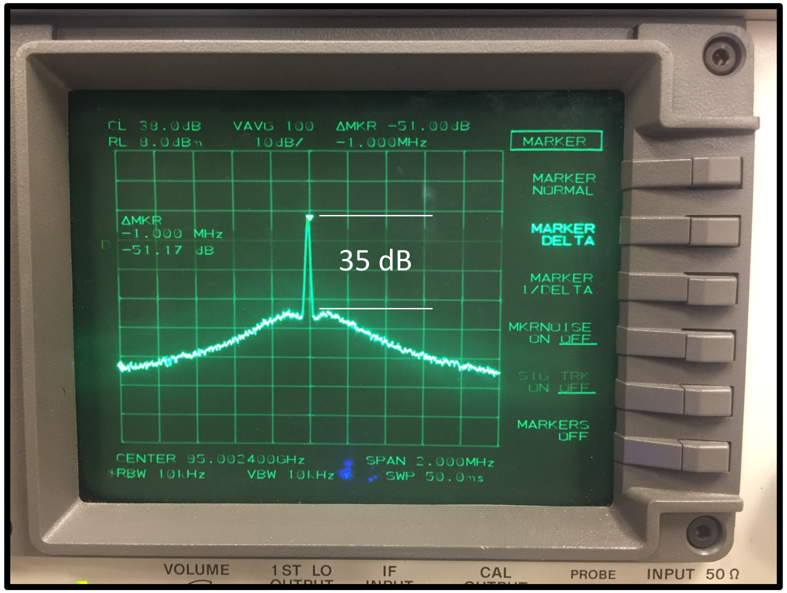
- Packaged in a self-contained module with USB interface (to set power/frequency) and access telemetry.
- Contains all regulators, power conditioning and a dedicated micro-controller to interact with the on-chip calibration algorithms.
- WR-10 output waveguide port for RF.

Output Power Performance



Spectral Quality and Phase Noise Performance





- ❖ **Phase noise corner is set by 1 MHz loop bandwidth of the internal PLL. Competitive with multiplied low-frequency sources, for a fraction of the DC power consumption.**

- ❖ **Spectral purity is high, no reference or fractional spurious components detected throughout the band.**

Thoughts to take away

- SWITCH is an exciting measurement concept that extensively uses CubeSat form factors making system size, weight and power very demanding.

- Leveraging commercial CMOS system-on-chip technology can provide the solution to these challenges while still delivering competitive performance.

- Need an industry standard approach to CMOS design and verification to be successful as modern SoCs are very complex with digital-assisted analog and background calibration.