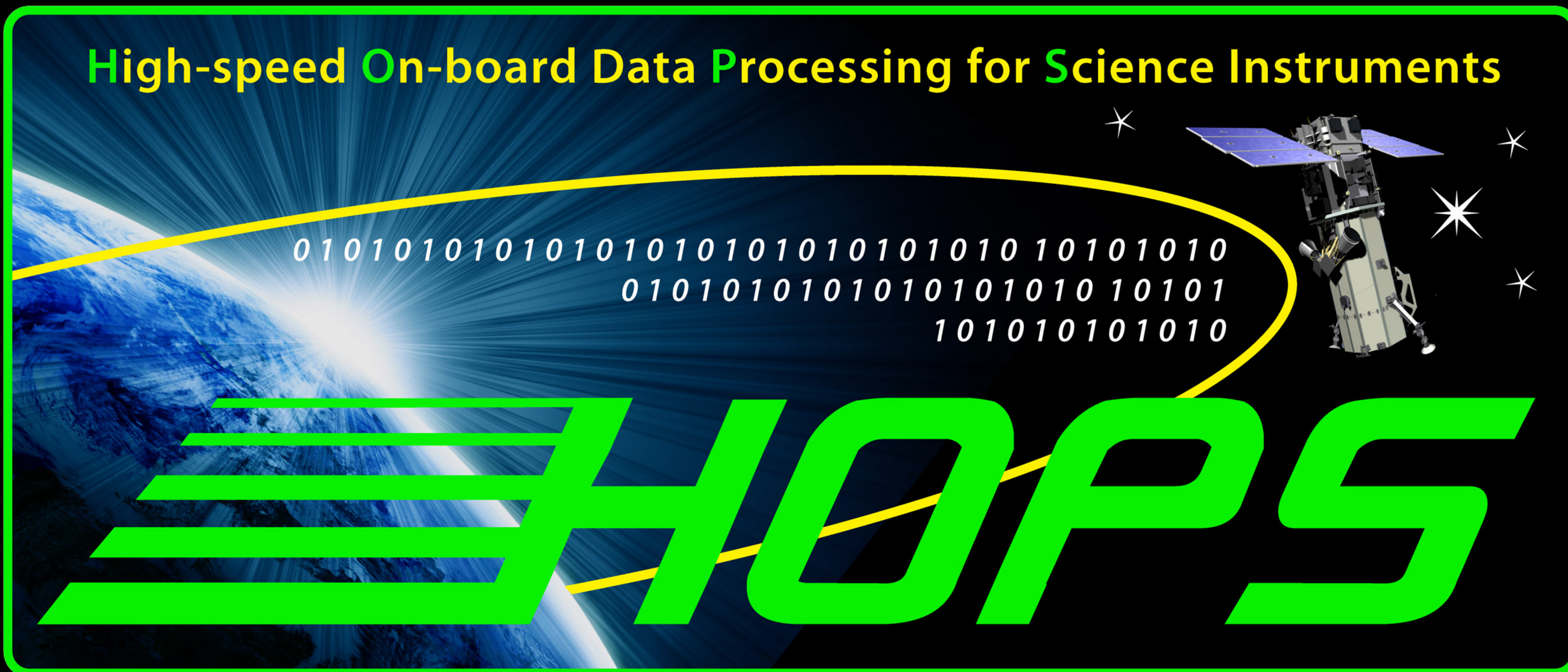


High-speed On-board Data Processing for Science Instruments (HOPS)

Drs. Jeffrey Beyon & Tak Ng

NASA Langley Research Center
Hampton, VA 23681

October 28, 2014

High-Speed On-Board Data Processing for Science Instruments (HOPS)

AIST-11-0007

Drs. Jeffrey Beyon & Tak Ng

NASA Langley Research Center
Hampton, VA 23681

October 28, 2014

Outline

- Introduction
- Personnel
- Uniqueness of HOPS
- Application of HOPS
- Integration of HOPS into Science Projects
- Impact
- HOPS – Concept to Flight
- HOPS HW Power Ratings (ASCENDS)
- HOPS Collaboration
- 2014 Flight Campaigns
- HOPS on the HU-25
- HOPS on the DC-8
- ESTO Collaboration and Team Work
- Acknowledgment and Q&A

Introduction

- Funded by NASA's ESTO (Earth Science Technology Office) AIST (Advanced Information Systems Technology) program.
- Period: April, 2012 – March, 2015
- Entry TRL 2, Exit TRL 5.

- Goals
  - Develop a high-speed, on-board reconfigurable and scalable data processing platform for science instruments
  - Demonstrate HOPS capabilities to address computationally intensive ASCENDS, ACE, and 3-D Winds algorithms.
    - ASCENDS: Active Sensing of CO2 Emissions over Nights, Days, and Seasons
    - ACE: Aerosol Cloud Ecosystems
  - Demonstrate HOPS is reconfigurable and scalable.

- Risk reduction in advancement to TRL-6.
  - Components with flight-ready equivalents.
  - Board layout and packaging will adhere to the flight standard.
  - Printed circuit boards will accommodate the flight component or its commercial equivalent.

Introduction

- HOPS is an enabler for science mission with extremely high data processing rate.
  - ASCENDS: Replace time domain with frequency domain processing and make real-time data processing possible.
  - 3D Winds: Real-time high resolution range wind profiling with fast Fourier transform.
  - ACE: Fast Bore-sight alignment.

- HOPS is reconfigurable and scalable with quick turn-around time.
  - Extremely high memory and inter-board bandwidths.
  - Plug and play VHDL Cores.

- HOPS is path-to-flight.
  - HOPS proto-type with COTS (HOPS COTS) has proven its superb data rate handling capabilities.
  - HOPS custom board hardware (HOPS HW) is path-to-flight.
  - HOPS development path offers risk and cost reduction to space flight.

- Two successful flight campaigns with HOPS COTS
  - End-to-end demonstration with ACES (ESTO IIP) on the HU-25 in July, 2014.
  - End-to-end demonstration with ASCENDS instrument on the DC-8 in August, 2014

Personnel

Name	Title	Organization	Task or Activity
Dr. Jeffrey Beyon	PI	NASA LaRC	Lead researcher, algorithms and wind lidar, project management
Dr. Tak-Kwong Ng	Co-I	NASA LaRC	HOPS module lead developer
Mr. Wallace Harrison	Co-I	NASA LaRC	ASCENDS algorithm lead
Dr. Bing Lin	Co-I	NASA LaRC	ASCENDS signal processing lead
Dr. Yongxiang Hu	Co-I	NASA LaRC	ACE algorithm lead
Dr. Edward Browell	Collaborator	NASA LaRC	ASCENDS algorithm support
Dr. Michael Kavaya	Collaborator	NASA LaRC	3-D Winds DAWN Air algorithm support
Dr. Alan George	Collaborator	Univ. of FL	FPGA development support
Dr. Robert Hodson	Collaborator	NASA LaRC	HOPS module development support

Uniqueness of HOPS

- State-of-the-art (SOA) on-board processing
  - SpaceCube at GSFC.
  - flight board Aitech S950 3U cPCI Radiation Tolerant PowerPC Single Board Computer (SBC)

- How is HOPS different from the current SOA systems?
  - Goal: To meet critical data processing requirements of ASCENDS and 3-D Winds, and further science projects in general by reducing data rate
  - New Approaches different from the current systems
    - FPGA/Memory bandwidth approaching 16 GB/sec
      - Maximum processor-to-SDRAM bandwidth: 132 MB/sec*
    - Inter-board communication bandwidth approaching 4 GB/sec
      - Maximum processor-to-cPCI bandwidth: 132 MB/sec*
    - Plug & play VHDL cores for the easy and efficient implementation of ASCENDS and 3-D Winds, and other similar algorithms.

    - *SOA flight board Aitech S950 3U cPCI Radiation Tolerant PowerPC Single Board Computer (SBC)

Uniqueness of HOPS

- Reconfigurable, Scalable and Reusable
  - FPGA
  - Modular by boards. 4 boards proposed in the HOPS proposal.
  - Plug & play VHDL cores for the easy and efficient implementation of ASCENDS, 3-D Winds, ACE, and other similar algorithms
  - Common IP cores, reusable user-friendly computational elements

- Path-to-flight technology
  - Flight board design rules
  - Components with flight equivalent

- Bus
  - cPCI-Bus: for slower tasks such as controls, data products, etc.
  - Xilinx IP core with Rocket IO Transceivers: for inter-board connection

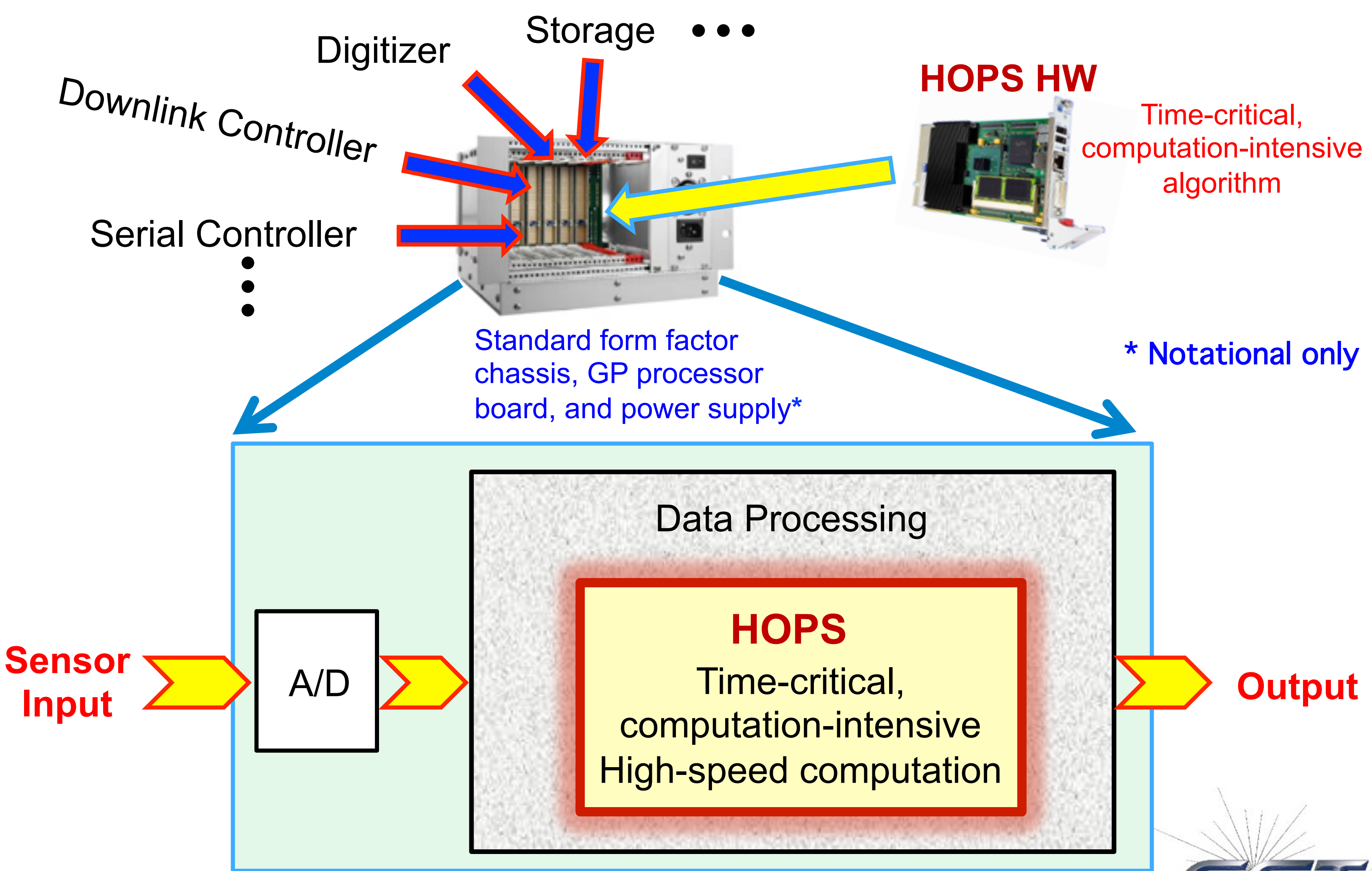
Application of HOPS

	Data In Sample Counts	Data Out Sample Counts	Reduction Rate	
ASCENDS	8,388,608*	24	99.99%	In = 64K @ 64Hz, 2 ch Out = 12 ratios, 2 ch
3-D Winds	1,100,000	179	98.36%	In = 55,000 @ 20Hz Out = 179 peaks

* Twice the ASCENDS airborne requirement which is 4 Million Samples (MS) per second (2 MS/channel, 2 channels total). 13,107,200 samples at 100 Hz have tested successfully and presented at the first annual review. HOPS COTS data processing rate is far greater. (at least 20 MS/sec for two channels)

- This table accounts for essential and meaningful science data products for further processing.
- HOPS can be reprogramed if algorithm needs to change for different science needs.

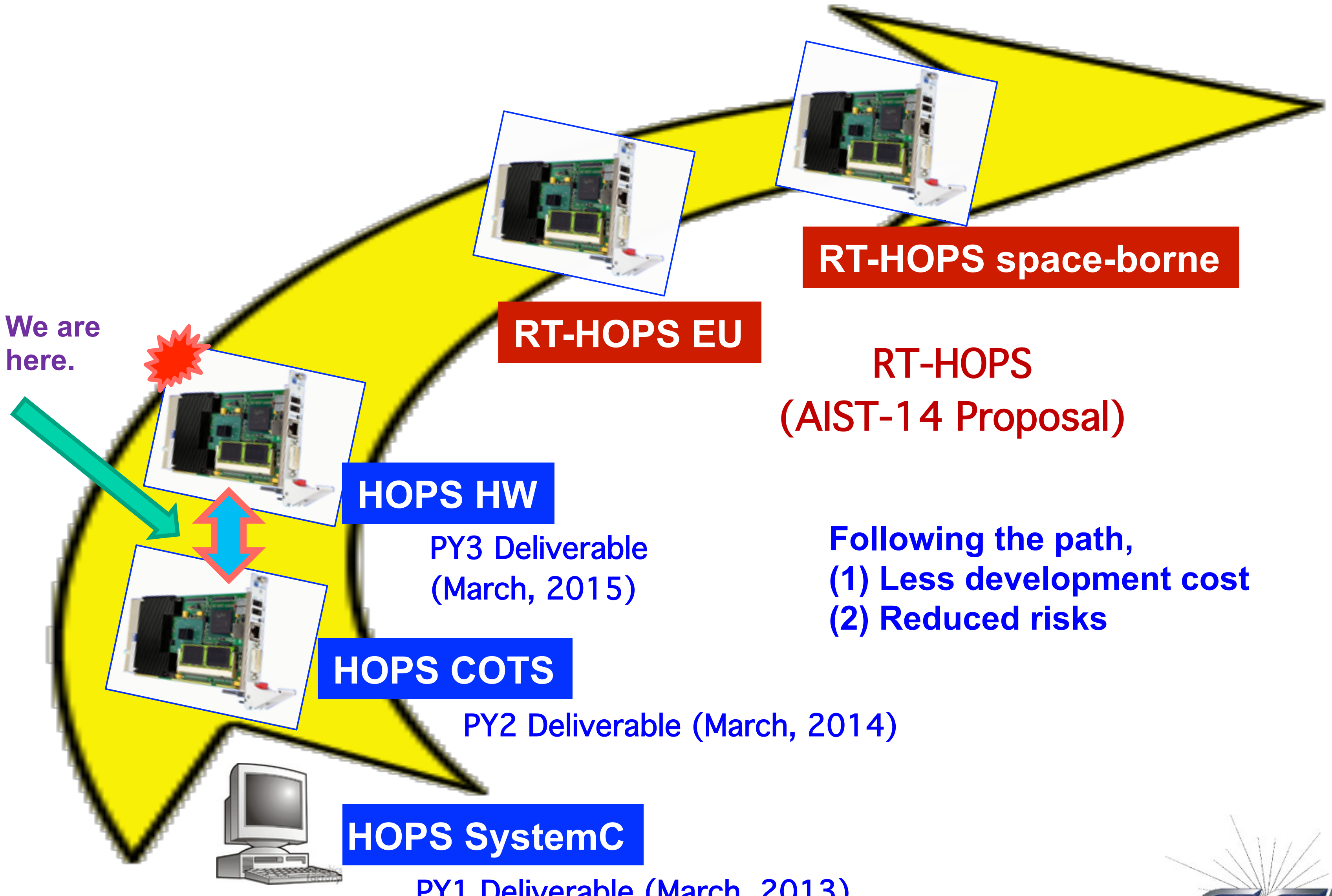
Integration of HOPS into Science Projects



Impact

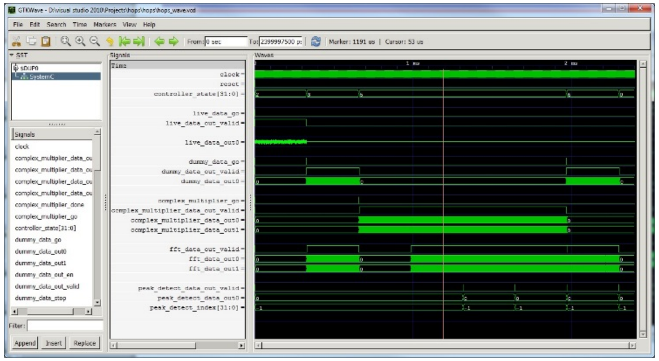
- HOPS Exit TRL 5 and path-to-flight components ensure successful transition to TRL 6.
- Reconfigurable hardware platform tailored for science instruments.
- VHDL cores with common interface shorten the development of critical high speed processing components demanded by mission science.
- Data rate reduction and real-time processing enabling science missions. (ASCENDS, 3D Winds (DAWN), and ACE in particular for the project HOPS)
- Advancing the SOA on-board processing technology via collaboration with the science and engineering teams and academia focusing on critical Decadal Survey missions.

HOPS – Concept to Flight



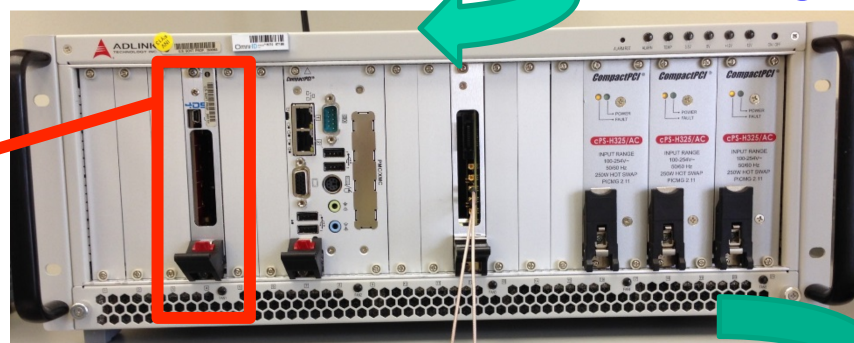
Following the path,
(1) Less development cost
(2) Reduced risks

HOPS – Concept to Flight

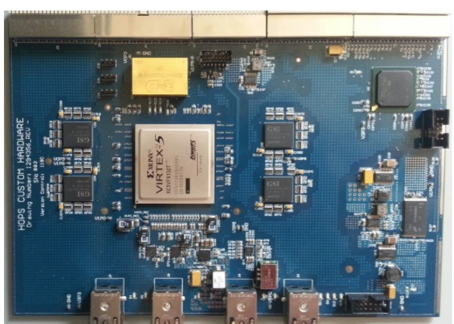


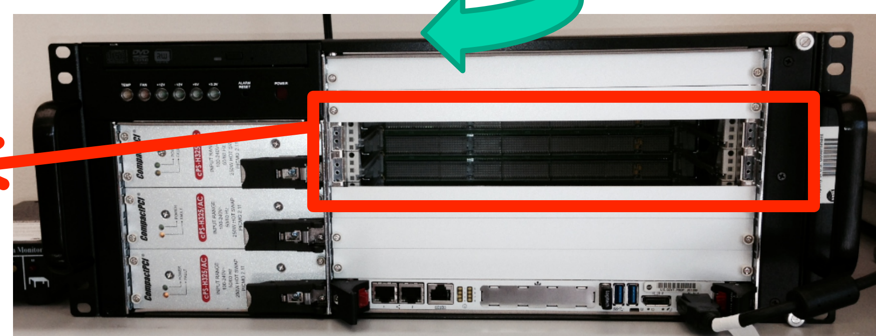
SystemC

HOPS COTS (3U)



HOPS HW (6U)





HOPS HW Power Ratings (ASCENDS)

	SOA RT 1 GHz GPP PowerPC 750FX	HOPS HW and RT-HOPS HW
Samples/sec	< 0.151 MS/sec	> 18 MS/sec*
Board Qty for Equivalent Performance	120	1
Power (Watt)	1,440	12 (HOPS HW)** 30 (RT-HOPS)***
Mass (lb.)	82.8	1.38
Cost	$24 Million	$20K (HOPS HW) $350K (RT-HOPS HW)

- * Lower bound running ASCENDS algorithm. 3-D Winds not shown due to its lower requirements.
- ** HOPS HW 12W proposed in HOPS proposal. Actual rating will be available in December, 2014. HOPS HW and RT-HOPS use different Virtex 5 for higher power rating for RT-HOPS.
- *** AIST-14 proposal submitted in June, 2014.

HOPS Collaboration

- LaRC science teams: ACES and ASCENDS
- LaRC Engineering Directorate branches: Thermal and Mechanical
- Other NASA centers and contractors
  - Kennedy Space Center (KSC): Joint proposal effort discussion
  - Armstrong Flight Research Center (AFRC): HOPS COTS integration in the DC-8.
  - Exelis Inc. HOPS COTS flight demonstration with MFLL instrument.
- Academia
  - University of Florida (UF) in Gainesville: NSF CHREC (Center for High-Performance Reconfigurable Computing)
  - University of Michigan (UM) in Ann Arbor
  - Summer intern students: 1 in 2013 and 3 in 2014 (UF and UM)

2014 Flight Campaigns

- Flight demonstration of HOPS COTS with (1) ASCENDS CarbonHawk Experiment Simulator (ACES) and (2) Exelis Inc. Multifunctional Fiber Laser Lidar (MFLL) Instrument
  - ACES: ESTO Instrument Incubator Program (IIP) for March, 2011 – March, 2014.
    - PI: Dr. Michael Obland
    - Aircraft: HU-25 based at LaRC in Hampton, VA.
    - To advance technologies critical to measuring atmospheric column CO2 mixing ratios in support of ASCENDS
    - ACES provides two channels of science data and HOPS COTS system process them real-time.
  - MFLL Instrument: The predecessor of ACES system. O_2 portion funded by ESTO Advanced Component Technology (ACT). Has flown since 2005 in support of ASCENDS. Built jointly by LaRC and Exelis Inc. (ITT).
    - LaRC PM: Byron Meadows
    - Exelis Inc. Lead: Dr. Jeremy Dobler
    - Aircraft: DC-8 based at AFRC in Palmdale, CA.

2014 Flight Campaigns

HOPS Flight Campaigns	Campaign 1	Campaign 2
Location	LaRC in Hampton, VA	AFRC in Palmdale, CA
Aircraft	HU-25	DC-8
Period	July 1st – 16th	July 27th – August 22nd
Real-Time On-Board Data Rate	4 million samples per second. 14-bit fixed point per sample.	
Algorithm	ASCENDS	
Flight Hours*	~ 11.7 hours	~ 11 hours
Data Hours**	20:43:34	14:58:34
Science Team	ACES (ESTO IIP)	Exelis Inc. (ESTO ACT)
Goals	*See next slide.*	

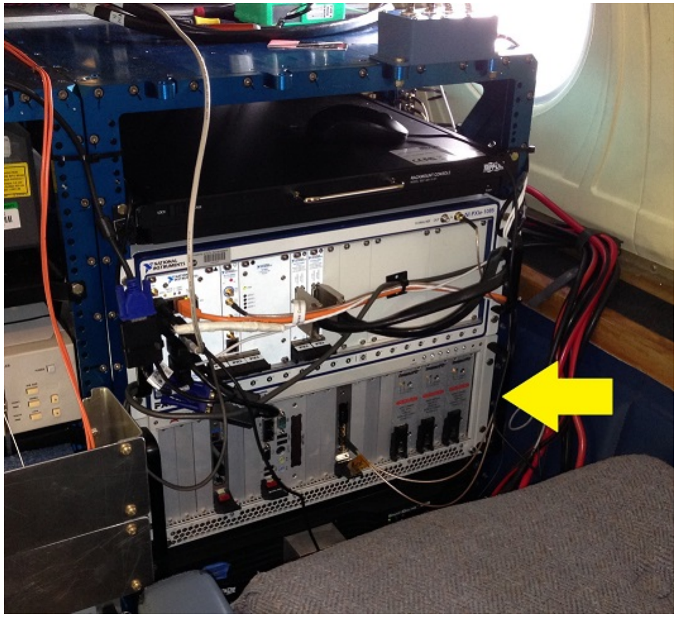
* With an operator aboard. HOPS COTS is quasi-autonomous.
** Some data sets were acquired without an operator aboard.

2014 Flight Campaigns

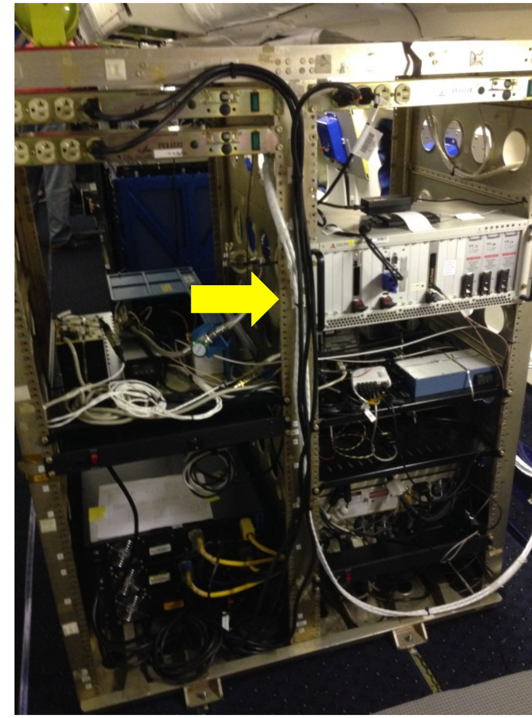
	Campaign 1	Campaign 2
Goals	- Learn from a small aircraft campaign to prepare for the DC-8 campaign. - Check the integration of HOPS COTS in a 3U cPCI system with a COTS digitizer. - Check HOPS COTS functionality. - Check the integration of HOPS into a project and identify any issues. (cabling, boot-up sequence, power management, data archive, HOPS system monitoring, etc.) - Test the sample code that utilizes HOPS COTS with a digitizer. - End-to-end demonstration.	Goals in campaign 1 plus - Apply lessons from Campaign 1 to a larger platform DC-8. - Check the heat dissipation of FPGA on the DC-8 during the mission. - Check integration issues with a larger platform. - End-to-end demonstration.

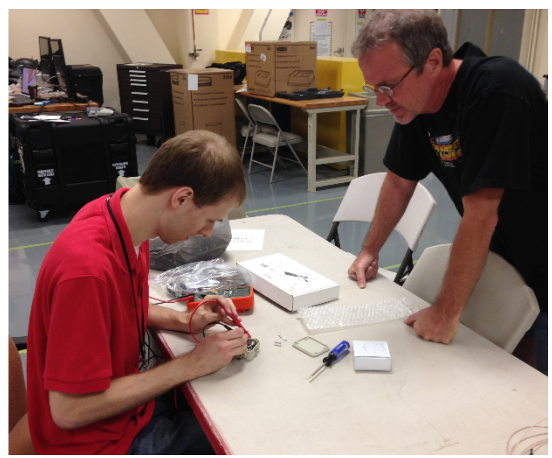
Earth Science Technology Office

HOPS on the HU-25



HOPS on the DC-8





ESTO Collaboration and Team Work

*ESTO ACT (MFLL) – ESTO IIP (ACES) – ESTO AIST (HOPS)

* O_2 portion only.

Acknowledgments

We are very grateful for the support from

NASA Science Mission Directorate (SMD),

NASA SMD Earth Science Technology Office (ESTO),

and the ESTO Advanced Information System Technology (AIST) program.

Acronym List

- ACE: Aerosol-Cloud-Ecosystems
- ACES: ASCENDS CarbonHawk Experiment Simulator
- ACT: Advanced Component Technology
- ASCENDS: Active Sensing of CO2 Emissions over Nights, Days, and Seasons
- CHREC: Center for High-Performance Reconfigurable Computing
- COTS: Commercially Off The Shelf
- DSP: Digital Signal Processing (Processor)
- EU: Engineering Unit
- FPGA: Field-Programmable Gate Array
- GP: General Purpose
- GPP: General Purpose Processor
- HOPS: High-Speed On-Board Data Processing for Science Instruments
- HOPS HW: HOPS Hardware. aka HOPS custom board. Final deliverable.
- IIP: Instrument Incubator Program
- IT: Integration and Testing
- MFLL: Multifunctional Fiber Laser Lidar
- MS: Million Sample
- PI: Principal Investigator

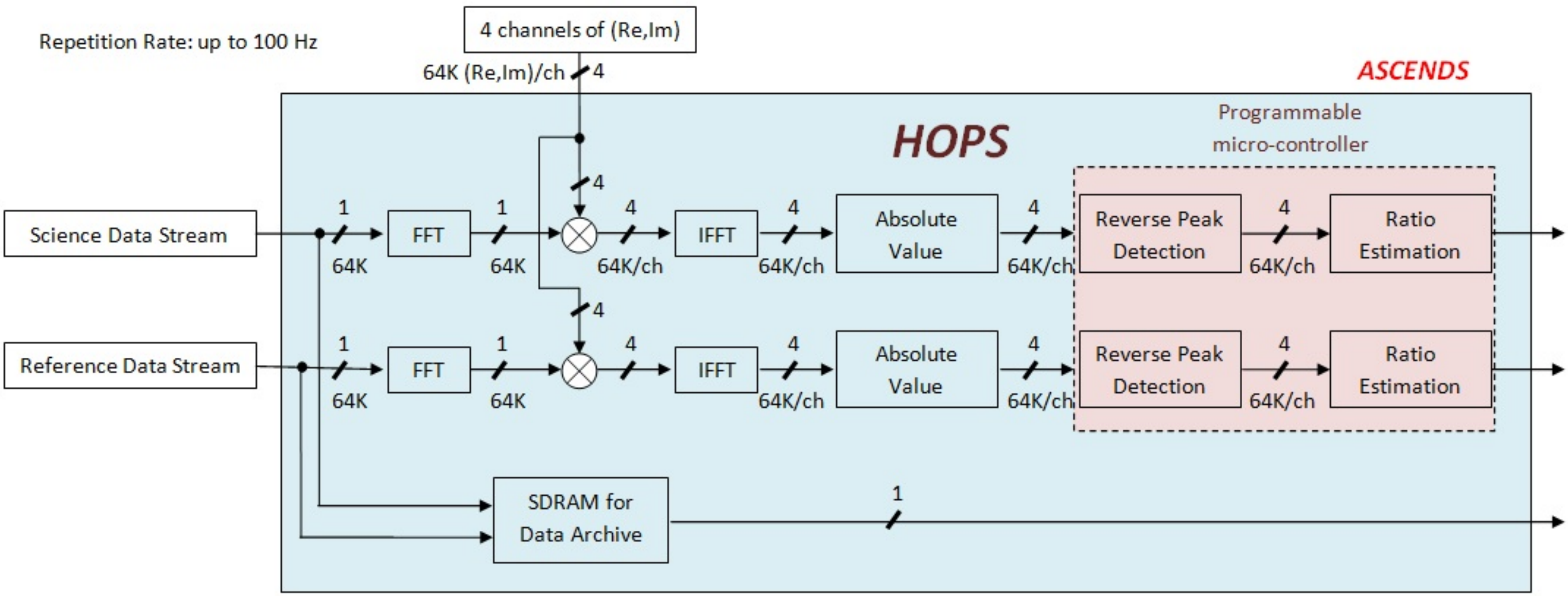
Acronym List

- PM: Project Manager
- PY: Phase Year or Project Year
- RT-HOPS: Radiation Tolerant HOPS
- SBC: Single Board Computer
- SDRAM: Synchronous Dynamic Random-Access Memory
- SOA: State-Of-The-Art
- TRL: Technical Readiness Level
- UF: University of Florida
- UM: University of Michigan
- VHDL: VHSIC Hardware Description Language

BACKUP

Mapping of Algorithm onto HOPS

- HOPS for ASCENDS



Earth Science Technology Office

Mapping of Algorithm onto HOPS

- HOPS for 3-D Winds