Modeling and Fabrication of a Nano-multiplication-region Avalanche Photodiode

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***Abstract*-A nano-multiplication-region avalanche photodiode (NAPD) featuring confinement of a multiplication region and a charging region in a nano-pillar was proposed for realization of novel near-constant-gain mode multiplication, low dark count rate, low afterpulsing and high avalanche initiation probability. Process and device simulations showed that near-constant-gain mode multiplication can be realized in NAPD with a properly doped charging layer. Prototype NAPDs were built with a feasible processing technology. First I-V characteristics of NAPD with plateau structures were observed.**

I. INTRODUCTION

Avalanche photodiode (APD) arrays have attracted a lot of interest in recent years because of their single photon detection based capability to perform ultra-low light imaging. Several APD arrays have been reported lately showing steady progress in dark count rate reduction, uniformity control and CMOS processing technology compatibility [1-4].

It is noticed that the hitherto reported APD arrays are solely realized on Geiger mode because the other avalanche mode, linear gain mode, is not suitable for array applications. Since a Geiger mode pixel cannot recognize the number of photons incident during a frame period, but a binary status instead, the dynamic range of the imaging array will be severely limited. Avalanching pixel employing charge integration can be a solution [5], but it requires a bias-independent gain characteristic that has not been demonstrated.

The nano-multiplication-region avalanche photodiode (NAPD) presented here[†] was designed to provide a third avalanche mode other than the traditional Geiger and linear gain modes, i.e., a near-constant-gain or constant-gain mode multiplication. A nano-multiplication-region and a charging layer confined in a nano-pillar will enable the novel mode by introducing a feedback mechanism. With such a feedback, inner self-quenching will occur immediately following an avalanching event and then cap the gain at a certain value. Fig. 1 (a) shows an idealized gain characteristic based on our simulations. With such a step-like function, a pixel as shown in Fig. 1 (b) that is similar to that of CMOS imaging sensor [6] but with two gain statuses can be constructed. By switching the bias of a NAPD between HV for a certain gain and LV for a gain of unity, imaging from ultra-low light through bright illumination can be fulfilled using one array, resulting in very high dynamic range.

[†] This work is fully sponsored by NASA/APRA under JPL task NMO710834

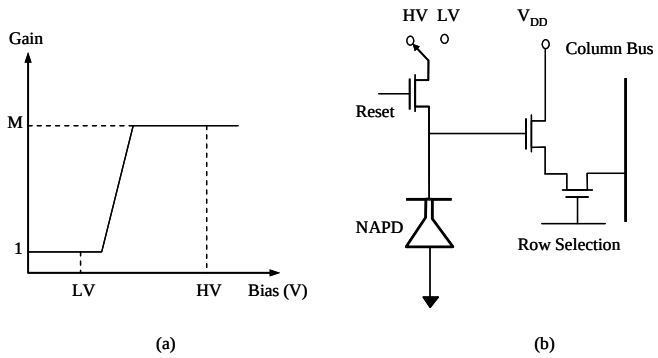

Fig. 1. (a) Constant gain characteristic of NAPD based on simulation results and (b) A two-status charge integration pixel circuit enabled by the constant-gain mode multiplication.

The other benefits from the structural innovation include reduced dark count rate [7], very low afterpulsing probability and high avalanche initiation probability, which are all important factors to a high dynamic range and high signal-to-noise ratio imaging array [8]. In this paper, structure and process of the NAPD are described in section II. Modeling for fabrication process and device performances are presented in section III. Results of the first test of prototype NAPDs are displayed in section IV, and a conclusion of the initiative work are given in section V.

II. STRUCTURE AND PROCESS

Shown in Fig. 2 is the schematic structure of the nano-multiplication-region avalanche photodiode.

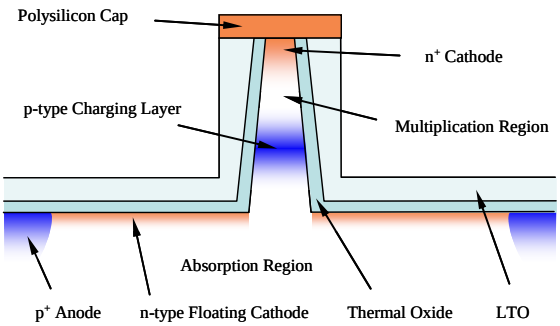

Fig. 2. Schematic diagram of the NAPD structure.

A. *Structure*

As shown in Fig. 2, an NAPD can be seen as composed of two portions, a photoelectron collector constituting a n-type floating cathode and an absorption region beneath it, and a nano-pillar which contains a charging layer, a multiplication region and a heavily doped n-type cathode. The floating cathode can help extension of the depletion region to the edge of the detector for high speed and high quantum efficiency photoelectron collection. The photoelectrons collected by the floating cathode will further move into the nano-pillar and trigger avalanche events in sequence. The nano-pillar has a typical height of 800-1000 nm and a typical average diameter of 100 -150 nm.

B. *Principle of Inner Quenching*

Discussed below in this sub-section is an analysis which suggests that constant-gain mode multiplication is an intrinsic avalanching mechanism of a NAPD.

An important fact is that the holes generated in an avalanche event have to move through the charging layer on their way out of the pillar and back to the anode. As it will be depicted later in this paper, the shallow potential well in the charging layer will lead to temporary accumulation of holes in the charging layer and simultaneous reduction of the net space charge of the charging layer because the holes hold opposite charges to that of the charging layer. The resulting reduction of the multiplication field, ΔE, can be estimated using the following equation,

$$\Delta E \approx e\Delta N /(\varepsilon_0 \varepsilon_{Si} A), \quad (1)$$

where e is the electron charge, ΔN is the number of holes accumulated in the potential well, ε_0 and ε_{Si} are the permittivities of vacuum and silicon, and A the cross sectional area of the nano-pillar. According to (1), for a nano-pillar of a diameter of 100 nm, 100 holes in the charging layer will reduce the field by 1.94×10^5 V/cm, which is about 15-20 % of the avalanching field of silicon. Since carrier multiplication is very sensitive to the magnitude of the field and the multiplied holes can easily exceed the assumed number of 100, we believe that the field modulation by the multiplied holes can be strong enough to quench sequential avalanche events and, as a result, exhibit a constant or near constant gain.

C. *Process of Fabrication*

P-type silicon wafers with resistivity of 80 Ω-cm were used for fabrication of prototype NAPDs. EBL (Electron Beam Lithography) and ICP RIE (Inductively-Coupled-Plasma Reactive-Ion-Etching) were employed to define the nano-patterns of nano-pillars and form the nano-pillars, respectively. The SEM photographs shown in Fig. 3 display some nano-pillars obtained in the process.

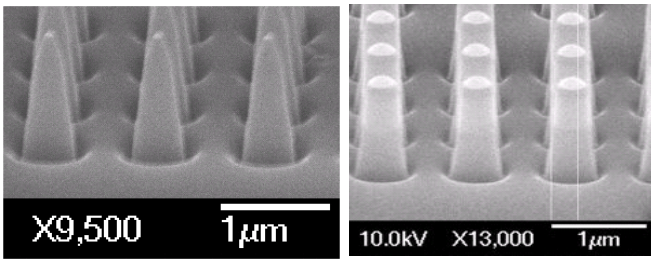

Fig. 3. SEM pictures of nano-pillars of different original patterning sizes. The achieved aspect ratio is about 5.

The wafers are then thermally oxidized for the dual purposes of passivation and pillar size thinning. The diameter reduction of the nano-pillars due to the oxidation was about 60 nm. Boron implant was followed to form the n-type floating cathode on the shoulder area of the wafers. Near one micron thick LTO (Low Temperature Oxide) was then deposited on the wafers and CMP (Chemical Mechanical Polishing) was employed to planarize the surface and expose the tips of the nano-pillars. Next was deposited a 120 nm thick polysilicon layer for nano-pillar contact and interconnection between the tips of the nano-pillars and their outside wirebonding pads. Implants of boron and phosphorus were then performed in sequence to form the charging layer and the cathode, respectively. Lithography was executed to define the elevated leads between the nano-pillars and their wirebonding pads on the polysilicon layer. ICP RIE etches were performed to remove the polysilicon and most of the LTO layer outside the pillar-lead-pad areas. Boron implant for anode was then proceeded following lithographic definition of the anode areas. After rapid thermal annealing at 900° C for 10 minutes, contacts to cathodes and anodes were opened using lithography and wet etch. Metal interconnection and pads were finally formed using lithography, electron-beam evaporation and RIE etching.

A photograph of a resulted NAPD device is shown in Fig. 4. The device shown there is composed of eight guard NAPDs and a central NAPD with pixel dimensions of 200 μm × 200 μm and average pillar diameter of 100-150 nm. While the nine NAPDs share a common anode (but with more then one peripheral pad in order to meet the requirement of JPL's high-frequency probe test system), the central NAPD has a separate cathode and the eight neighboring NAPDs have one common cathode. Both the cathode leads are at an elevated height level with the top of the nano-pillars.

III. PROCESS AND DEVICE SIMULATIONS

The fabrication process and device performances of a cylindrical NAPD with the nano-pillar along the central axis were simulated using SILVACO's software ATHENA and ATLAS.

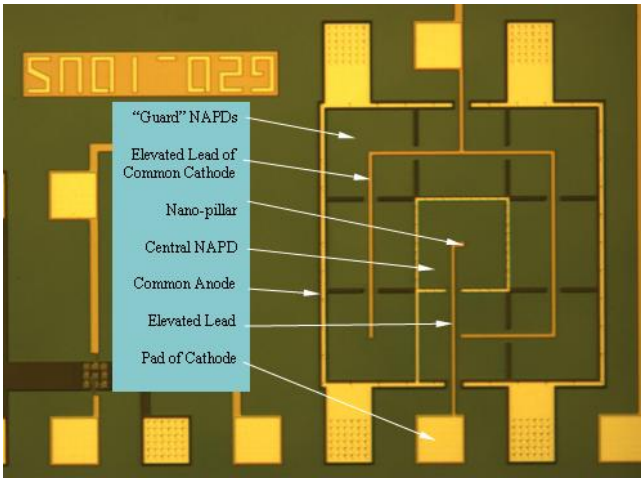

Fig. 4. A microscope photograph of a fabricated NAPD device. The common cathode of the guard NAPDs and the cathode of the central NAPD, both at an elevated height level with the top of the nano-pillars, are applied with equal bias in the test to ensure that the dark current from the outside area into the central NAPD can be eliminated. Thw width of the photograph is about 1400 μm.

A. *Depletion of Absorption and multiplication Regions*

A typical simulation result of depletion in the absorption region and in the nano-pillar is displayed in Fig. 5. Real structural and processing parameters were used for the simulation. The boron dose of the charging layer was $5\times10^{13}/cm^2$. The bias applied on the cathode was 20 Volts and the simulated potential of the floating cathode was 5.4 Volts. While the thick depletion layer in absorption region is evidently seen in Fig. 5, simulation on another structure without the n-type floating cathode showed that only a limited region close to the nano-pillar was depleted there.

B. *Doping of Cathode and Charging Layer*

Doping profiles along the axes of the nano-pillars with different charging layer doses were simulated and the results are displayed in Fig. 6.

C. *Band Structures*

The band structures corresponding to the different doping profiles shown in Fig. 6 were simulated and the results are displayed in Fig. 7. A potential well of hole is seen for each of the band diagrams. It was found that charging layer with doping dose below $5\times10^{12}/cm^2$ would be completely depleted. Therefore, these charging layers are indeed reach-through structures that have been widely incorporated in traditional APDs [9]. On the other hand, according to the simulations, charging layers of heavier doping could not be completely depleted. An interesting result is that an undepleted charging layer will lead to constant gain over a wide bias range while a depleted charging layer will not.

D. *I-V Curves*

Reverse I-V characteristics of NAPDs with different charging layer doses were simulated and the results are shown in Fig. 8.

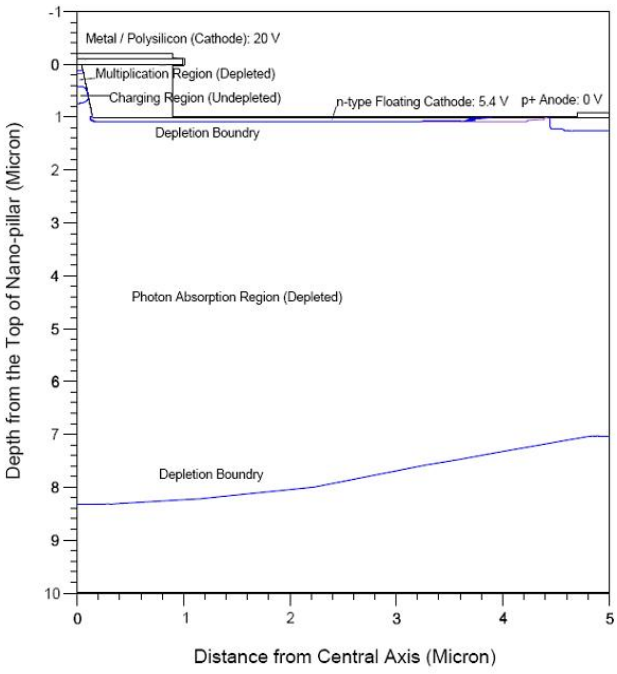

Fig. 5. Depletion simulated in a cylindrical NAPD with real structural and processing parameters, including the aspect ratio of the nano-pillar.

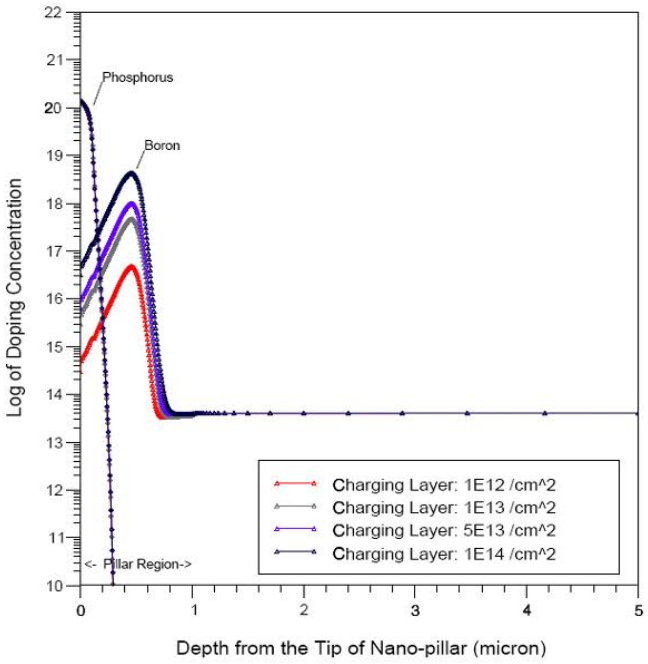

Fig. 6. Simulated doping profiles of NAPDs with different charging layer doses. The implant energy and dose for the cathode and the implant energy for the charging layer are 55 KeV, $2\times10^{15}/cm^2$ and180 KeV, respectively, for all the doping structures.

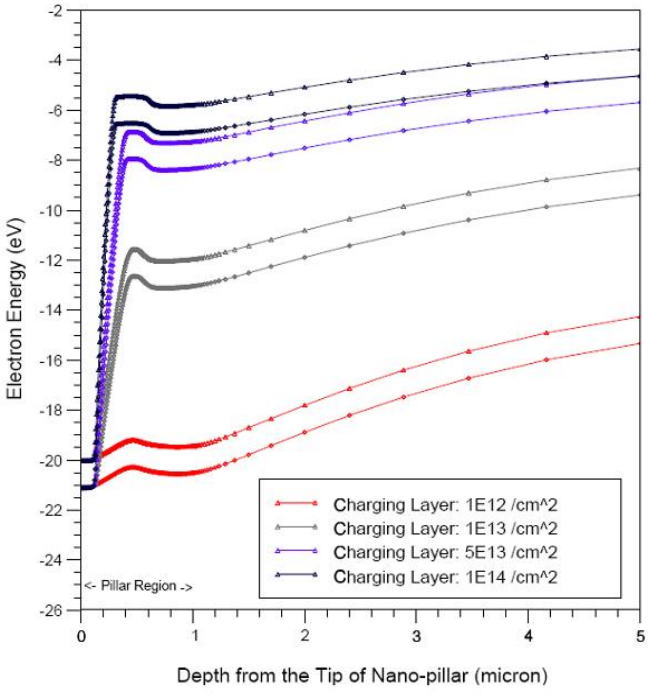

Fig. 7. Band diagrams simulated for different charging layers doses.

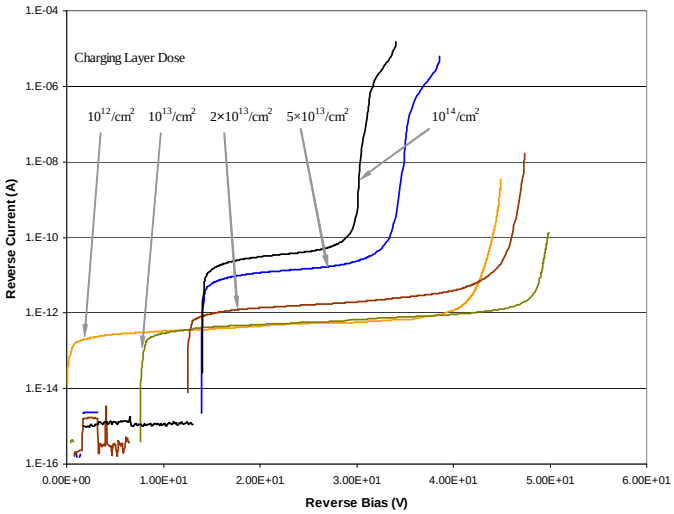

Fig. 8. Simulated reverse I-V curves for NAPD devices with different charging layers doses.

Among the reverse I-V characteristics shown in Fig. 8, the first curve (charging layer dose 10^{12}/cm^2) is like the I-V curve of a standard p-n junction. The magnitude of the reverse current represents the generation-recombination dark current of the device. The next curve (charging layer doping 10^{13}/cm^2) exhibits clear "reaching-through", i.e. the depletion region reaching into the absorption region, at about 8 V. The next three curves (charging layer doping 2×10^{13}/cm^2, 5×10^{13}/cm^2, and 10^{14}/cm^2) all show a reach-through-like step and the reverse currents beyond the reach-through points are obviously larger than the dark current. By examining the recombination components and impact ionization components at different biases and different locations, it was concluded that the magnified reverse currents between the "reach-through" points and the final breakdown were caused by carrier multiplication.

E. Gain

Gain curves were extracted and are shown in Fig. 9.

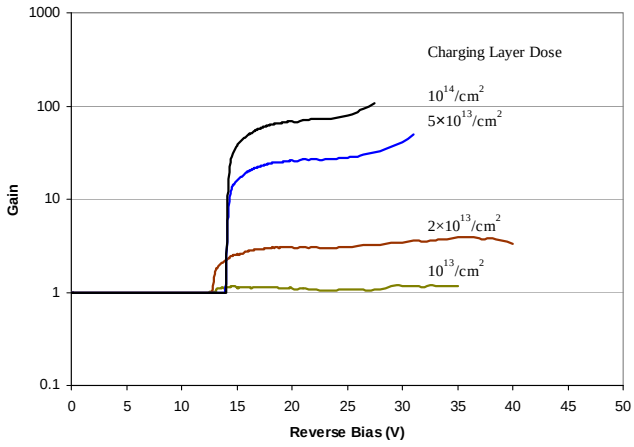

Fig. 9. Near-constant-gain characteristics obtained from simulations for devices with different charging layer doping doses.

Near-constant gain characteristics over certain bias ranges were obtained and displayed in Fig. 9. Since the carrier impact ionization coefficients used for the simulations have not been calibrated with experiments, the gain curves displayed in Fig. 9 only depict qualitative dependences of the gain on the bias and charging layer dose.

IV. TEST

Two 100 μm ×100 μm prototype NAPDs (NPD01 and NAPD02) with charging layer doping of 5×10^{13}/cm^2, nano-pillar diameter of 100 nm and nano-pillar height of 800 nm were tested using a probe station and HP 4145B Semiconductor Parameter Analyzer. The obtained I-V curves are displayed in Fig. 10 in both logarithm and linear scales. The curves can be divided into three segments: the pre-reach-through stage, the gain stage, and the final breakdown stage. The high noise observed in the pre-reach-through stage is thought of to be from the probe station. The slow breakdown seen in the third segment was probably due to the current compliance protection of HB 4145B.

The experimentally obtained I-V curves have shown clear "plateau" structures in the second segments, which are similar to the "plateau" structure displayed in Fig. 8. For this reason, slowly varying gains over wide bias ranges are expected for NAPDs Further test is ongoing and new results will be reported.

V. CONCLUSION

A nano-multiplication-region avalanche photodiode (NAPD) was proposed for development of a constant-gain or near-constant-gain mode multiplication and other performance advantages. Existence of the constant gain mode multiplication in the proposed NAPD structure was supported by simulation results. Prototype NAPD devices have been successively built using a special and feasible processing technology developed in this work. I-V curves obtained from the prototype NAPDs showed "plateau" structures similar to our predictions. Based on this result, we have greater confidence that the devices we are preparing to manufacture will exhibit the properties we are seeking. However, there remains the possibility that the I-V curves as measured do not actually represent the expected gain characteristic. Further tests will be performed to answer if the near-constant gain mode is there or not definitively.

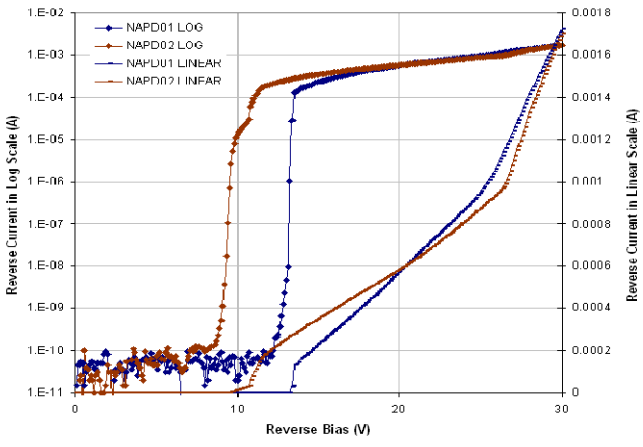

Fig. 10. I-V curves experimentally obtained from two NAPD devices, displayed in both logarithm and linear scales.

ACKNOWLEDGMENT

The authors would like to thank Mr. William Farr of Jet Propulsion Laboratory for helpful discussion on self-quenching and Dr. X. Wang of UCLA for her help in SEM observation.

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