

High Data Rate Receiver for Optical PPM Communications

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Abstract—A scalable receiver and distributed decoder architecture for an optical receiver array is presented. A 150 Mbps receiver prototype and 60 Mbps SC-PPM decoder prototype are described and their incorporation into the JPL optical communications test-bed are shown.

I. INTRODUCTION

In a deep space optical communications link, the limited transmit power and extended distances will require the receiver to operate in a photon starved regime [1]. Under these conditions, large effective receiver apertures, achieved through the use of an optical receiver array [2], photon counting detectors [3], and powerful error-correcting codes [4] are used to enable high data rate communications. A scalable receiver and distributed decoder architecture for an optical pulse position modulation (PPM) signaling scheme using an inter-symbol guard-time along with a Serially-Concatenated Pulse-Position-Modulation (SC-PPM) error correcting code will be presented. A hardware prototype implementation of a 150 Mbps, 16 PPM receiver and 60 Mbps SC-PPM decoder developed at the Jet Propulsion Laboratory and integrated within an optical communications test-bed is described. This prototype takes as input the electrical output from a photon counting detector and synchronizes and demodulates the PPM modulation producing estimates that are passed to a set of decoders that recover the transmitted information sequence in real-time. Finally, the receiver and decoder are shown operating in an end-to-end test-bed wherein real-time high definition video is captured, transmitted through free-space, detected, received, decoded, and displayed.

II. SCALABLE ARCHITECTURE

A scalable receiver and distributed decoder architecture for an optical PPM signaling scheme is shown in Figure 1. Each element of the array consists of an aperture, front-end optics, and a photon counting detector. Each pixel of the detector is followed by a receiver that independently synchronizes to the received signal and produces a set of PPM slot statistics [5]. The slot statistics from up to four receivers are combined in each slot accumulator. Outputs from multiple slot accumulators can also be combined allowing the architecture to be scaled to any number of array elements. The combined slot statistics are fed to the decoder where the transmitted information bits are recovered. The high data rate requires

multiple SC-PPM decoders. By creating a distributed decoding architecture, where each element contains a single SC-PPM decoder that when busy passes the undecoded codeword on to a subsequent decoder, an arbitrary throughput can be achieved by adding more elements. The receivers, slot accumulators, and distributed decoder elements are all connected using optical fiber and communicate using multi-gigabit serial deserializer (SERDES) small form pluggable (SFP) optical transceivers. The slot accumulator and distributed decoder elements differ only in their field programmable gate array (FPGA) programming and can be realized using a common hardware platform. The receiver while requiring the same digital hardware capabilities also requires analog front end processing.

III. PROTOTYPE

Custom hardware for the receiver and slot-accumulator/distributed decoder elements are currently being developed. Prototypes of the receiver and an SC-PPM decoder were implemented on commercial FPGA development boards and integrated into the JPL optical communications test-bed. Descriptions of the receiver and decoder prototypes follow.

A. Receiver

The hardware prototype implementation of a 150 Mbps, 16 PPM receiver is composed of a custom front end Photon-Discriminator-Deserializer (PDD) board and a commercial FPGA development board manufactured by Memec, model number FF1152. The FPGA board has a Xilinx XC2VP50 Virtex-II Pro FPGA and the digital processing algorithms implemented on it were programmed using the Verilog hardware description language. The functionality of the receiver can be categorized into three areas: detection, synchronization, and estimation.

The detection process produces estimates of the number of detector output pulses within a PPM slot time. Each detector output pulse represents either a photon arrival or a dark event and is received in the presence of a broadband thermal noise. To detect a pulse, the output voltage of the detector is compared to a threshold voltage forming a binary decision as to the presence or absence of a detector pulse. This operation is accomplished by the custom PDD board, using an Analog Devices ADCMP580 high-speed comparator

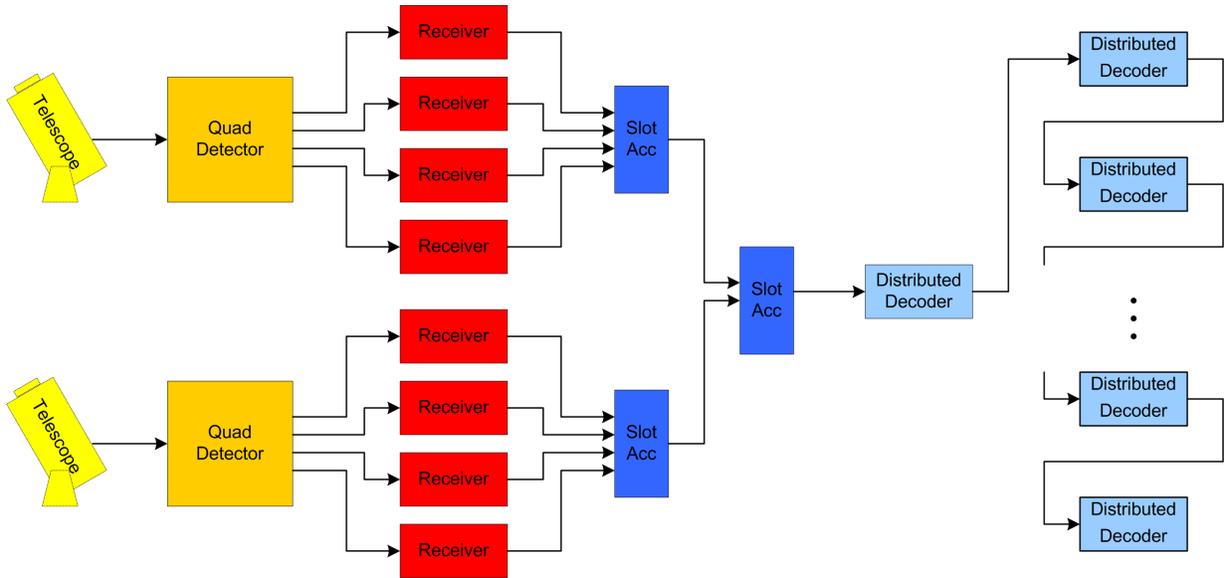


Fig. 1. Scalable Optical PPM Receiver and Distributed Decoder Architecture

chip. By clocking the comparator chip at rates up to 10GHz, a serial stream of binary decisions is produced. In order to process the serial data stream on the FPGA board, which operates at 200MHz, the serial data stream is parallelized by a factor of sixteen and transmitted using low-voltage-differential-signaling (LVDS) to the FPGA development board where digital processing is performed. As the output pulses of the optical detector have a duration spanning multiple decision periods, in order not to over count the number of pulses, an edge detection algorithm is applied to each vector of decisions; other detection algorithms can also be implemented to adjust for different optical detectors. The output of the edge detection algorithm is summed over each slot producing an estimate of the number of detector output pulses within a slot time. These slot statistics are the primary output of the receiver and are packetized and passed to the decoder through SERDES SFP transceivers for SC-PPM decoding.

In order to demodulate a PPM signal, the slot and symbol boundaries of the received signal must be determined. Due to the phase and frequency differences between the transmitter and receiver clocks, these boundaries are initially unknown and vary with time. The receiver must therefore acquire and synchronize to the slot and symbol clocks of the detected signal. In order to enable this synchronization, an inter-symbol guard-time is employed; this synchronization technique was chosen since it does not expend transmitter power and allows for low-complexity receiver implementations [6]. The inter-symbol guard-time is a period of no transmission between each symbol lasting a single slot time. By correlating the slot statistics against the empty slot, representing the inter-symbol guard-time, estimates of the symbol and slot boundaries are formed. The length of this correlation is varied depending on the operating conditions and affects both the fidelity of the estimates and their latency. Initial frequency acquisition is obtained by tracking the location of the inter-symbol guard-time slot in subsequent correlations. Phase and frequency

tracking of the slot and symbol clocks is performed by the slot synchronizer which uses the correlator outputs in a feedback loop with a second order loop filter. The bandwidth of the tracking loop is both a function of the correlator length and the loop filter parameters.

Estimation of the receiver operating point is necessary for the decoding of the SC-PPM code, where the probability of each slot statistic is calculated, as well as to calibrate the receiver and its performance. The average number of signal and background photon arrivals are used by the decoder in the generation of the slot likelihood ratios. These quantities are estimated by comparing the empty inter-symbol guard-time slot, composed only of background arrivals, with the other slots. Optimization of the receiver detection threshold and slot synchronizer parameters is performed using the inter-symbol guard-time error rate. This error rate is estimated by counting the number of times an inter-symbol guard-time slot has a greater slot statistic than the any of the other slots in that symbol. These estimates are used for monitor and control operations and in the case of the average signal and background counts also passed to the decoder.

B. Decoder

The SC-PPM decoder is implemented on a Nallatech BenNUEY PCI FPGA development board which resides in a personal computer (PC) running the open-source Linux operating system for monitor and control operations. The decoder receives input from the receiver via a pair of SERDES channels connected through Infiniband copper connectors. The decoded data is transferred to a National Instruments PCI-6561 capture card through eight LVDS channels where the data is then transferred through the PCI bus for capture or storage.

For each symbol, the decoder receives the slot statistics and channel operating point from the receiver via a pair of SERDES transceivers into a Xilinx XC2VP20 Virtex-II Pro FPGA. The log-likelihood ratio for each slot is formed and

a codeword of log-likelihoods are buffered for subsequent output to one of eight pipelined SC-PPM decoder cores [7]. In total, sixteen decoders are implemented on four Xilinx XC4VLX160 Virtex-4 FPGAs. The eight decoder pairs receive codewords in a round robin fashion. Each decoder iteratively decodes a codeword with a fixed number of iterations and then passes the decoded data to an output buffer. A codeword consists of 3780 symbols; the start of each codeword must be determined in order to pass a decoder the correct set of likelihood ratios. This codeword synchronization is accomplished by stepping through each of the 3780 symbol offsets until the cyclic-redundancy-check (CRC) of the decoded codeword passes indicating correct decoding. With code synchronization achieved, the decoded data is output onto eight LVDS channels.

IV. TEST BED INTEGRATION

The receiver and decoder have been successfully integrated into an end-to-end test-bed consisting of a Canon XL H1 high definition (HD) camcorder, a compact laser transmitter, transmit and receive optics, a photon counting optical detector, a receiver, and a decoder operating at a rate of 50 Mbps. The data being transmitted across the optical link begins with video capture at the HD camcorder, which transmits real time HD data over a Firewire connection to a PC at a data rate of 25 Mbps. The data rate is augmented to 50 Mbps by inserting pseudo-random data alongside the HD camcorder data. The PC takes the data stream and transmits it over a universal serial bus (USB) interface to the compact laser transmitter where forward error correction (FEC) encoding and 16-PPM with inter-symbol guard-time modulation occur on an onboard FPGA. After FEC encoding and data modulation, the laser transmits the signal across a free-space link where receive optics focus the beam of light onto a photon counting optical detector. The detector produces electrical pulses that are passed to the receiver.

The receiver front end PDD sampling board samples the detector output at a rate of 3.4 Gbps. The receiver detects, synchronizes, and estimates the incoming signal. Some of the operations are shown in Figures 2 through 4, which display real time screen captures of the graphical user interface controlling both the receiver and the decoder. In Figure 2, the receiver's slot synchronizer tracks out the transmitted signal. Note the white line in the "offset/frequency" window display the receiver's estimate of where the transmitted inter-symbol guard-time slot resides. Since the transmitter and receiver frequencies differ, the guard-time slot changes over time as displayed. The figure also shows other slot synchronizer parameters such as the bandwidth of the loop, along with statistics of the slot timing error. Figure 3 displays the correlation results that the receiver employs for synchronization. As shown, the first slot contains a lower amplitude compared to all other slots. This minimum corresponds to the location of the guard-time slot. Once the receiver obtains slot and symbol timing, the slot statistics are passed to the SC-PPM decoder. The decoder processes the data, and an example operating point is shown in Figure 4 where the decoder is operating at

50 Mbps. Using various colored lines, the figure also shows the estimates of codeword error rate averaged over different time intervals. Finally, the decoder passes the data to a PC that strips out the pseudo-random data and transfers the video data to the HDM500 MPEG decoder card made by Stradis. The resulting video is displayed on a 42" Panasonic plasma television completing the optical communications link.

V. CONCLUSION

A scalable receiver and distributed decoder architecture for an optical receiver array using a PPM signaling scheme with an inter-symbol guard-time along with an SC-PPM error correcting code was presented. A 150 Mbps receiver prototype and 60 Mbps SC-PPM decoder prototype were described and their incorporation into the JPL optical communications test-bed were demonstrated.

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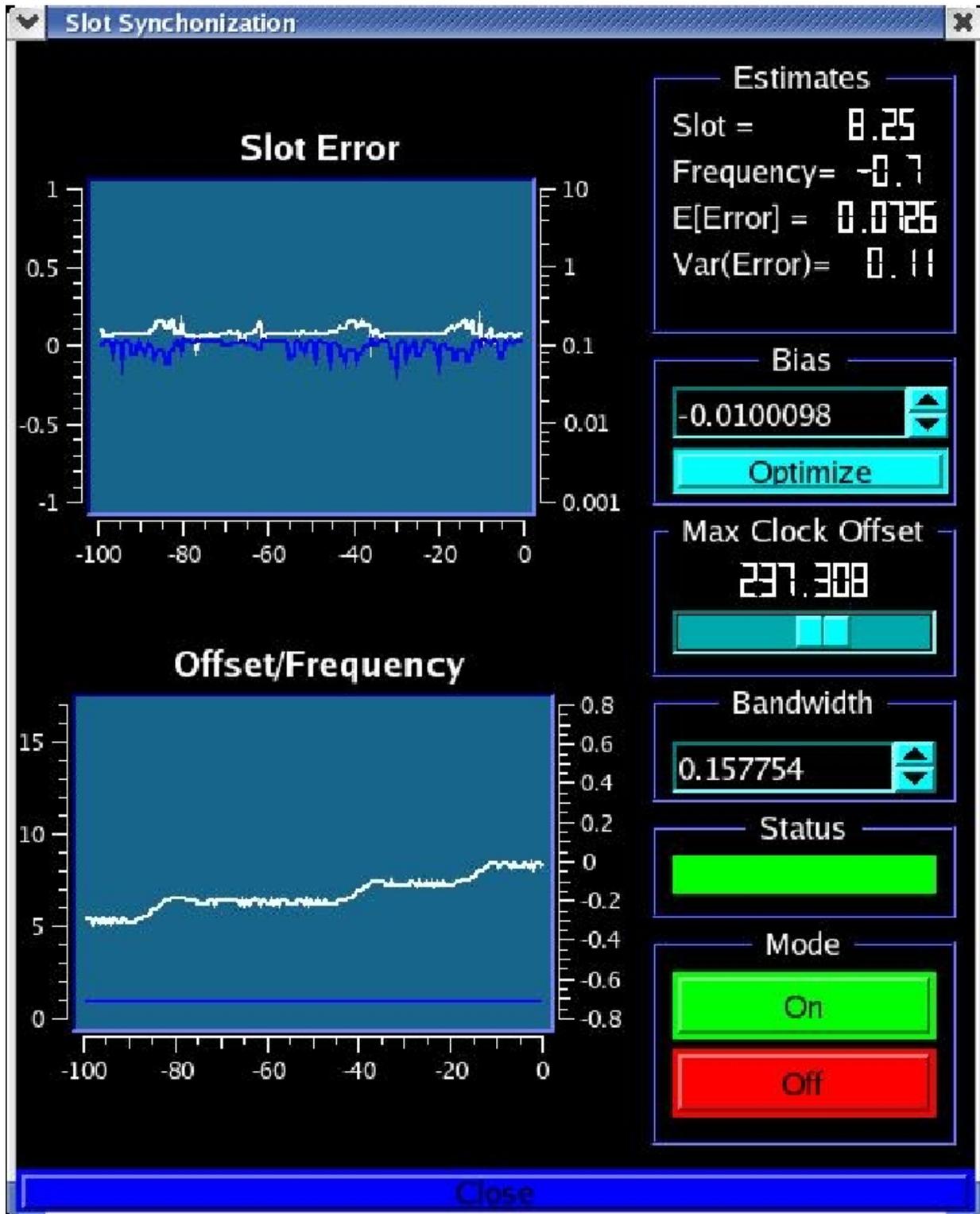


Fig. 2. Example of the receiver's slot synchronizer graphical user interface tracking the received signal.

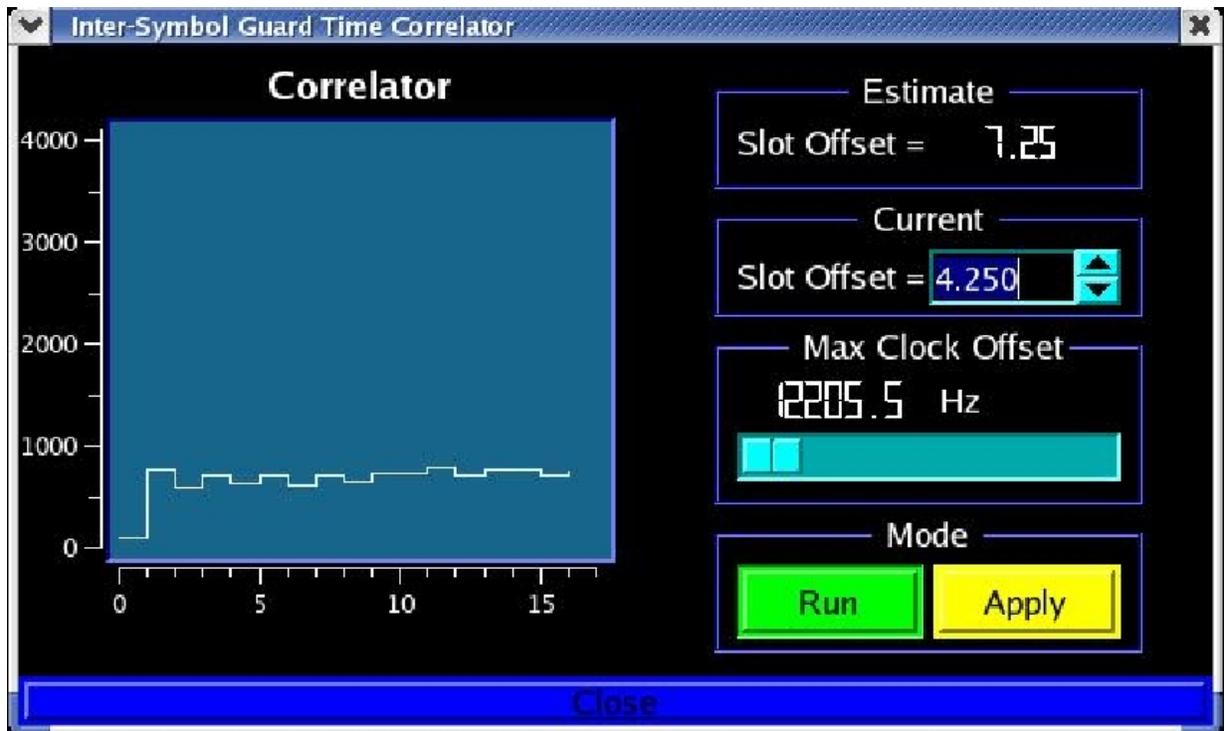


Fig. 3. Example of the receiver's correlator output displaying the inter-symbol guard-time slot.

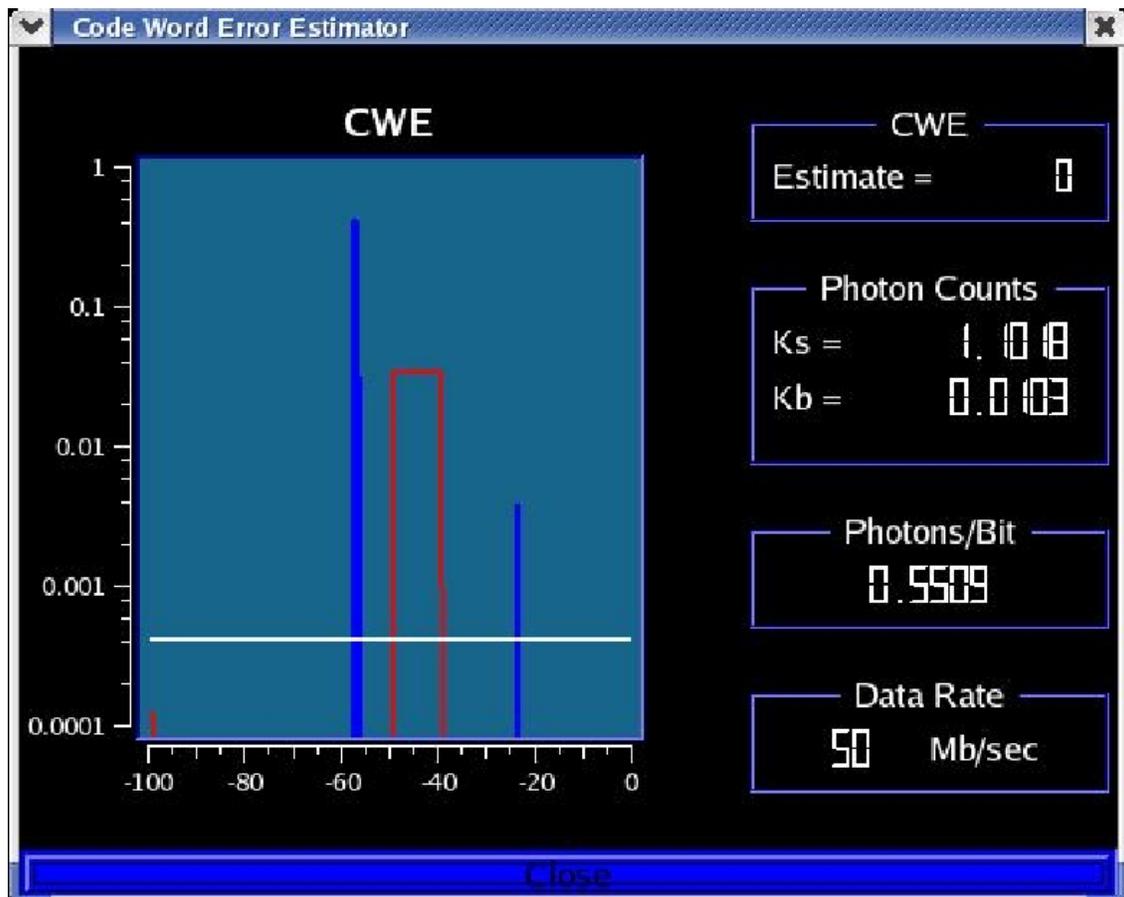


Fig. 4. The decoder codeword error rate performance operating at 50Mbps.