GeoSTAR-II

technology development and risk reduction for PATH

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Outline

• PATH Requirements Overview
• GeoSTAR: Synthetic Thinned Aperture Radiometry Demonstration
• GeoSTAR-II : Technology risk reduction for PATH mission
Precipitation and All-weather Temperature and Humidity (PATH)
Launch: 2016-2020
Mission Size: Medium

Sea surface temperature
Temperature and humidity profiles
Constraints on models for boundary layer, cloud, and precipitation processes

More accurate, longer-term weather forecasts
Improved storm track and intensification prediction and evacuation planning
Determination of geographic distribution and magnitude of storm surge and rain accumulation

PATH
High frequency, all-weather temperature and humidity soundings for weather forecasting and SST

GEO
 MW array spectrometer

$450 M

= GeoSTAR
PATH Requirements Flow

Requirements

Functional
T(z), q(z), L(z), TPW, LWC
SST, Precip (all weather)

Temporal
15 min updates

Spatial
50km/25 km

Mission Characteristics

50-183 GHz Bands
<0.3 K Retrievals

Geostationary orbit

Large Eff Aperture

Measurement Approach

Interferometer Approach

Technology Needs

Low Noise mm Devices

Low Power Correlators

Low Power Digitizers

Low Mass Receivers

Integrated system Demos

Mission Cost
Mass < 300 kg
Power < 300 W
No moving parts
Builds on ESTO’s Investments

All required component technology is now at TRL 5-6
System TRL is near 6

IIP98- MATHS
Key demonstrations:
- 90-140 GHz receiver modules
- 160-190 GHz receiver modules (TRL 5)

IIP03- GeoSTAR
Key demonstrations:
- 60 GHz modules
- FPGA based correlator
- Integrated STAR Array
- Imaging/sounding capability (TRL 6)

ACT06- MIMRAM
Key demonstrations:
- 180 GHz Noise (TRL 6)
- 180 GHz Integrated receiver (FY08-TRL 6)
Interferometric Array Receivers

Synthetic Aperture Interferometer: SMOS, GeoSTAR

Synthesizes images by correlating signals in the Fourier domain. All viewed pixels are simultaneously mapped. **No moving parts.**

\[
\Delta T(r,s) \equiv \left( \frac{\Omega \sqrt{1 - r^2 - s^2}}{A_u |f(r,s)|^2} \right) \frac{\pi}{2} \frac{T_s}{\sqrt{2\beta\tau}} 2n
\]

(No redundancy)

Example: \( T_{\text{sys}} = 1000 \text{K}, \) \( f = 200 \text{ MHz}, \) \( n = 300, \) \( N = 90000 \) then \( T = 47 \text{K-s}^{1/2}. \)
GeoSTAR Demonstrator Array

Demonstration prototype of a geostationary temperature and humidity sounder
24-Element Array Production

Receiver noise of 24 modules

Integrated module

Integrated Array

Noise Figure [dB]

Frequency [GHz]

0 1 2 3 4 5 6

50 51 52 53 54 55 56
Near Field measurement set-up

Near Field range

NF to FF transformation

\[
\hat{V}_{kj}^{FF} = V_{kj}^{NF} e^{-j k_0 (r_k - r_j)} e^{-j 2\pi (u\xi + v\eta)}
\]
4m Calibrator
GeoSTAR-II Objectives

- Develop 50 low-noise 183-GHz receivers
- Develop 3 2x8-element receiver sub-array modules
- Develop low-power Application-Specific Integrated Circuit (ASIC) correlator chips
- Develop low-mass/power signal distribution system
- Perform functional 183-GHz subsystem tests (not full imaging)
Design Refinement

Science driven requirement of 0.3 K NEDT forced a reexamination of system design.

4-row design improves sensitivity in critical field, decreases number of receivers, eases array density.
Low Noise Amplifiers
Converter Board Design

- Conversion gain 10 dB
- Power consumption <60mW
- Mass <3g
- Physical size .375”x.3”x.2”
Sub-Array Module

Manifold is structural basis of GeoSTAR sub-array which integrates:
- WR10 Local Oscillator distribution
- WR5 “twists” (+/- 60 degree and 0; unique to ea array)
- WR5 circular transitions
- all interfaces for IF PCBs, MIMRAM modules, horns, LO
“Tile” Hardware
High Speed Low Power ASICs

Correlator Proof of Concept

• Cross correlation for 3 arms of antennas
  – 17 antennas/arm
  – 2 signals/antenna (I/Q)
  – 2-bit signed
  – 3x17x2x1=102 digital antenna inputs

• Correlations per antenna pair
  – 4 (In*Im, In*Qm, Qn*Im, and Qn*Qm)
  – Antenna pairs on same arm not cross-correlated
  – Number of antenna pairs to be correlated
    3x17^2=867
  – Number of total correlations 4x867=3,468
  12 ASIC chips required
  – 3,468/12=289 correlations/ASIC

• 1GHz sample rate
• 1 second integration period
• 10msec accumulator readout
• 250uW/correlation at 1GHz
• Processed on TAPO IBM 90SL CMOS Initial tests look good
High Speed, Low Power ASICs

A/D Proof of Concept

- Assumptions:
  - 1GHz sample clock
  - 1V supply voltage
  - 40 µA current reference

- Input Common Mode Range \((V_{in+} + V_{in-})/2\)
  - 650mV – 850mV

- Differential Input Range \((V_{in+} - V_{in})\)
  - 200mV to +200mV

- 2 bit ADC, with independent threshold control
- 6 bit offset control for top and bottom thresholds
- 8 bit offset control for centre threshold
- LVDS output drivers
- SPI control bus
- 90nm digital CMOS process
## Performance Metrics

<table>
<thead>
<tr>
<th></th>
<th>Goal</th>
<th>CBE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Correlator</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>250 uW/corr</td>
<td>224 uW/corr*</td>
</tr>
<tr>
<td>BW</td>
<td>500 MHz</td>
<td>375 MHz</td>
</tr>
<tr>
<td><strong>Module Boards</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>15 dB</td>
<td>~10 dB</td>
</tr>
<tr>
<td>BW</td>
<td>165-183 GHz</td>
<td>165-183GHz*</td>
</tr>
<tr>
<td>Noise</td>
<td>400 K (3.7 dB)</td>
<td>~500K(4.3dB)</td>
</tr>
<tr>
<td>Power</td>
<td>42mW</td>
<td>60 mW</td>
</tr>
<tr>
<td><strong>Sub-Array Module</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mass</td>
<td>2kg</td>
<td>3.5 kg</td>
</tr>
<tr>
<td>Mech Tol</td>
<td>0.001”</td>
<td>tbd</td>
</tr>
<tr>
<td><strong>IF Subsystem</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mass (harness)</td>
<td>20 kg</td>
<td>~15 kg</td>
</tr>
<tr>
<td>BW</td>
<td>&gt;500 MHz</td>
<td>&gt;1 GHz</td>
</tr>
<tr>
<td>Gain</td>
<td>&gt;40 dB</td>
<td>&gt;40 dB</td>
</tr>
<tr>
<td>Power</td>
<td>0.94 mW/dB</td>
<td>0.69 mW/dB</td>
</tr>
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</table>
Summary

NASA has made steady progress on PATH Technologies

- Imaging capability has been demonstrated at 50-60 GHz
- Compact receiver technologies demonstrated up to 183 GHz
- ASIC Technologies (correlators and A/D) are being tested
- Key array technologies being demonstrated
- 183 GHz subsystem demonstration by end of year