On-Board Processor for Direct Distribution of Change Detection Data Products

Yunling Lou, Scott Hensley, Charles Le, Delwyn Moller
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive, MS 300-243
Pasadena, California 91109
Email: yunling.lou@jpl.nasa.gov

Abstract -- **We are developing an on-board imaging radar data processor for repeat-pass change detection and hazards management. This is the enabling technology for NASA ESE to utilize imaging radars. This processor will enable the observation and use of surface deformation data over rapidly evolving natural hazards, both as an aid to scientific understanding and to provide timely data to agencies responsible for the management and mitigation of natural disasters. Many hazards occur over periods of hours to days, and need to be sampled quickly. The new technology has the potential to save many lives and millions of dollars by putting critical information in the hands of disaster management agencies in time to be of use.**

The processor architecture integrates two key technologies by combining a Field Programmable Gate Array (FPGA) front-end with a reconfigurable computing back-end. Through this approach we are able to capitalize on the strengths of both technologies for the optimization of performance while maintaining flexibility where needed within the algorithmic implementation. A searchable on-board data archive will store the reference data sets needed for change detection processing. In this paper, we will present an overview of the change detection processing algorithm and the preliminary hardware architecture.

I. INTRODUCTION

Solid Earth studies have recently relied on repeat-pass interferometric synthetic aperture radar (InSAR) to map topographic deformation related to earthquakes [1,2]. Scientists believe that the deformation due to aseismic strain may be utilized for earthquake forecasting [3]. SAR data have also been used to detect land cover change due to vegetation growth, harvesting, forest fires, and logging, which contribute directly to the global carbon cycles [4]. Recently, hydrologists have used SAR data to monitor river level changes [5], flooding, snow melting, freeze/thaw boundaries, and soil moisture [6]. All these applications are research objectives of the NASA Earth Science Enterprise and are based on the comparison of two or more SAR data sets acquired over time. There is an urgent need to deliver change detection data products to the users expediently, especially in hazards and disaster management. Having the coherent and incoherent change detection data processing capability on-board a spacecraft, UAV, or aircraft not only saves time, but also eliminates the raw data downlink bottleneck and expensive ground processing facilities. It allows the mission operators to re-task the radar when necessary based on the results of the change detection data products. The benefit of this technology development is not limited to future Earth Science Enterprise imaging radar missions, but is the enabling technology for future planetary imaging radar missions where downlink data rate on the order of 10 Mbps is the limiting factor in high resolution radar imaging.

We have been funded by NASA's Earth Science Technology Office (ESTO) to build an on-board imaging radar data processor for change detection and hazards management under the 2002 Advanced Information System Technology (AIST) program. We began the processor development in July 2003 and are in the requirements and processor architecture definition phase. In this paper, we will describe the change detection processing algorithm, the processor requirements, and the preliminary hardware architecture based on the throughput and memory requirements of the processor. We will conclude the paper with our development plan.

II. CHANGE DETECTION PROCESSING ALGORITHM

We are developing an on-board processor for repeat-pass change detection (CDOP) for an L-band InSAR. The operational flow of the on-board processor is shown in Figure 1. There are two major functional blocks in the CDOP, the SAR processing block and the change detection processing block. SAR processing is done in parallel for the raw data set that is being collected and the reference raw data set collected in a previous data pass. This approach is chosen because the required on-board storage for raw data is much smaller than processed single-look complex data. SAR processing consists of range compression of the raw radar data, resampling to a reference trajectory (motion compensation), and azimuth compression into focused SAR imagery. Change detection processing combines the latest SAR imagery with a reference SAR imagery that was collected and processed during or after a previous pass. There are two types of change detection: incoherent change detection and coherent change detection. Incoherent change detection looks for changes in the intensity images that could be attributed to changes in soil moisture,

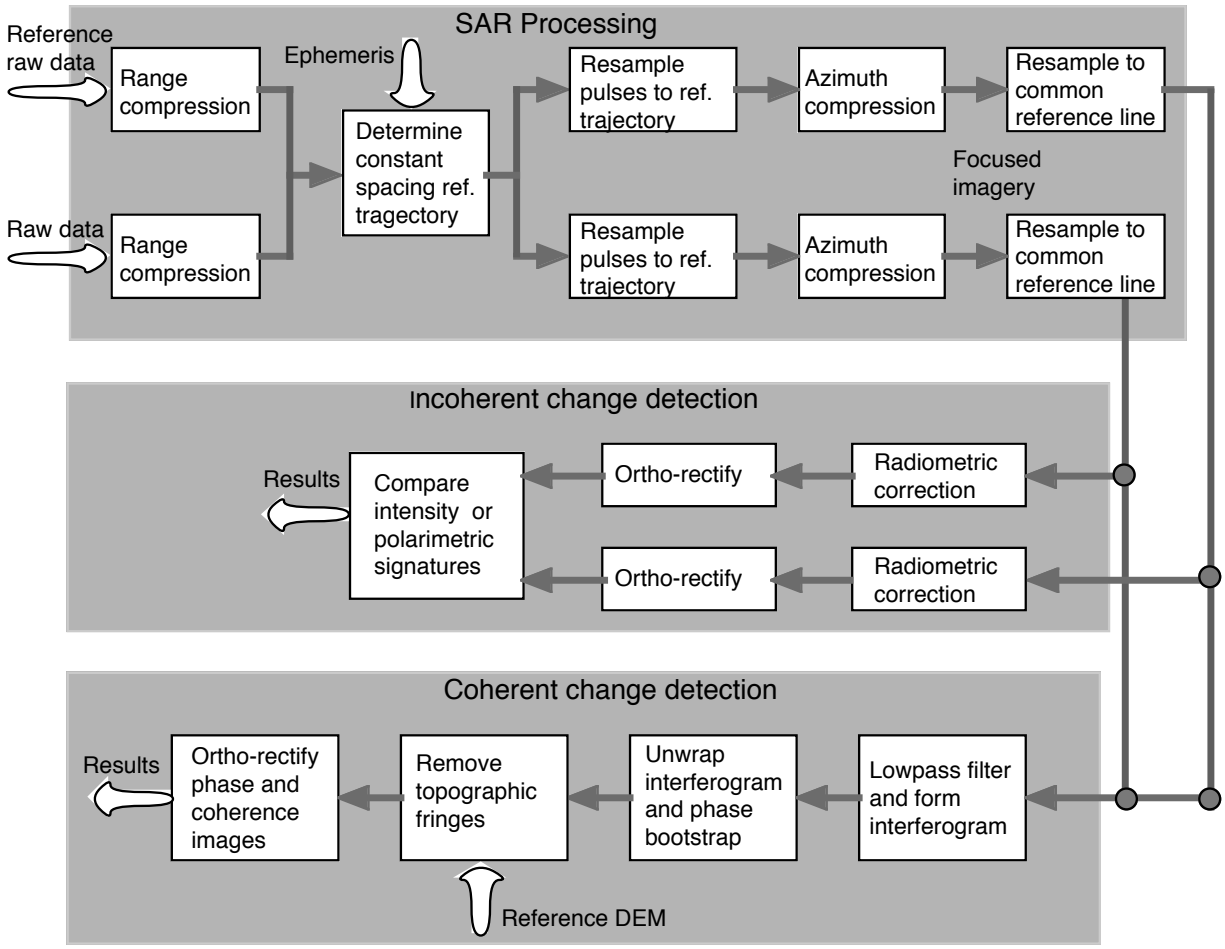

Figure 1. The operational flow of the CDOP.

vegetation growth, ground freezing or thawing, flooding, etc. Coherent change detection looks for changes in the phase data that are attributed to geophysical changes over time such as topographic deformation related to earthquakes and glacial motion. Coherent change detection is also called repeat-pass interferometry and is much more difficult to perform on-board the aircraft or spacecraft because of the complexity of the operations involved in co-registering the two data sets, phase unwrapping the interferogram, removing the topographic fringes, and ortho-rectifying the data to map coordinates.

The proposed CDOP will perform SAR processing in real-time and, as a goal, produce change detection data products with less than 3 minutes latency. The reason for this approach is as follows: a ground station typically has visibility of the spacecraft for about 12 minutes from horizon to horizon. If this ground station is placed at the center of the target site to receive data from both the ascending and descending passes, then the spacecraft has up to 6 minutes to process and downlink the results upon imaging the target site. With a processing latency of 3 minutes or less, the CDOP will have sufficient time to process the data collected up to a minute beyond the target site, which is about 430 km away assuming a typical low Earth orbit mission. This leaves the spacecraft with up to 2 minutes to downlink the results, which should take less than a minute assuming a 105 Mbps downlink.

III. PROCESSOR REQUIREMENTS

We plan to utilize an airborne radar system as a test-bed to validate the CDOP. The candidate airborne system is an unmanned airborne vehicle-based repeat-pass interferometric SAR system (UAVSAR) being developed under the NASA ESTO Instrument Incubator Program (IIP). The UAVSAR is an L-band (24 cm wavelength) 80 MHz bandwidth radar that will operate at an altitude of 13,700 m. The antenna is 0.5 m by 1.5 m and illuminates a range swath that extends from 20° to 60° off nadir. The system parameters are listed in Table 1. Based on the system parameters for this radar, the end-to-end processor throughput requirement is 2.4 GFLOPS (giga-floating point operations per second) and the memory requirement is 4.5 GB. The overall input/output data rate of the processor is about 500 Mbps. We will use the processor requirements to determine the hardware architecture and size the FPGAs and the microprocessor capabilities.

Table 1. System parameters of the UAVSAR.

Parameter	Value
Range Bandwidth	80 MHz
Sampling Rate (Offset Video)	180 MHz
Pulse Length	30 μs
Azimuth Samples per Patch	16384
Azimuth Reference Function	5850
Maximum Data Window	144 μs/7720
Azimuth Resolution	0.75 m
Range FFT Size	32768/16384
Number Valid Range Samples	7720
Interpolator Length	8
Smoothing Window Size	5
Presum Ratio	2
Antenna Length	1.5 m
Wavelength	24 cm
Range Pixel Size	1.66 m

The candidate spaceborne system used to size the real-time processing requirements for the CDOP spaceborne application is the European Space Agency (ESA)'s ESA Remote Sensing Satellite (ERS) radar. This radar is a C-band (5.6 cm wavelength) system flown at an altitude of 780 km in a 98° inclination angle orbit. The near and far range look angles of the swath are 17° to 23° which correspond to an approximate 100 km swath on the ground. The system parameters are listed in Table 2.

Table 2. System parameters of the ERS C-band radar.

Parameter	Value
Range Bandwidth	15.55 MHz
Sampling Rate (IQ)	18.96 MHz
Pulse Length	37.1 μs
Azimuth Samples per Patch	8192
Azimuth Reference Function	1024
Maximum Data Window	316 μs/6000
Azimuth Resolution	2.9 m
Range FFT Size	8192/8192
Number Valid Range Samples	6000
Interpolator Length	8
Smoothing Window Size	5
Presum Ratio	1
Antenna Length	12 m
Wavelength	5.6 cm
Range Pixel Size	7.90 m

Preliminary estimate based on the system parameters for this radar indicates that the overall throughput rate requirement is 13 GFLOPS and the memory requirement is 2 GB. The overall input/output data rate of the processor is about 2 Gbps. The processor throughput rate and data rate requirements will dictate the size and number of FPGAs we need to implement the image formation processor whereas the throughput rate and memory requirements will dictate the microprocessor card selection for the change detection processing task.

III. PROCESSOR HARDWARE ARCHITECTURE

To achieve real-time SAR processing and near real-time change detection processing, we will utilize a hybrid architecture that combines both the FPGA technology and the distributed microprocessor technology. The functional block diagram of the hardware architecture of the CDOP is shown in Figure 2. The computations for SAR image formation are highly regular, repetitive, and require little software control. They consist mainly of FFTs, matrix and vector multiplications, and convolutions. However, they are intensive, demanding over 70% of the required throughput and large memory bandwidth. In contrast, interferometric processing is heavily data-dependent with many conditional jumps and irregular data movements. A hybrid architecture can provide both the high performance of the FPGA technology as well as the programmable capability of the microprocessor to ensure an optimal hardware/software solution. This architecture is optimal in the sense of maximum throughput with minimum size, weight, and power. Other factors, such as the overall cost (including non-recurring engineering cost), time from development to deployment, ease of implementation, upgradability, and scalability, will also influence the choice of a potential hardware platform and its associated design methodology.

We have conducted a market survey and evaluated the commercial off-the-shelf (COTS) processor cards with a combination of high speed FPGAs and embedded PowerPC processor chips to perform the entire CDOP task. These cards are populated with the Xilinx Virtex-II Pro FPGAs with a large number of programmable logic devices and embedded multipliers for data-independent, computationally intensive tasks such as SAR image formation. However, the limited on-board memory (512 MB or less) and the relatively slow processing speed of the embedded PowerPC 7410 RISC-core processors prevent us from using these cards for the CDOP task. Ultimately, we determined that the best approach is to develop customized FPGA cards with sufficient on-board memory for the image formation processing and procure a separate, high speed multiprocessor card with 4 to 8 GB on-board memory for the interferometric processing (change detection processing) task. The multiprocessor card (or system) will utilize a high-speed backplane such as the 266 MB/s switch-fabric RACE++ for interconnectivity within the system and with the FPGA cards. The multiprocessor system will not only provide the large memory needed for change detection processing but also the flexibility for algorithm development and the capability of scaling with requirements and overhead. This flexible approach will allow the change detection processor to support a number of spaceborne radar missions with different change detection data products. We envision that the change detection processing task can be optimized with less memory usage and migrated to an FPGA platform with embedded microprocessors in the future for a specific spaceborne mission with specific output data products.

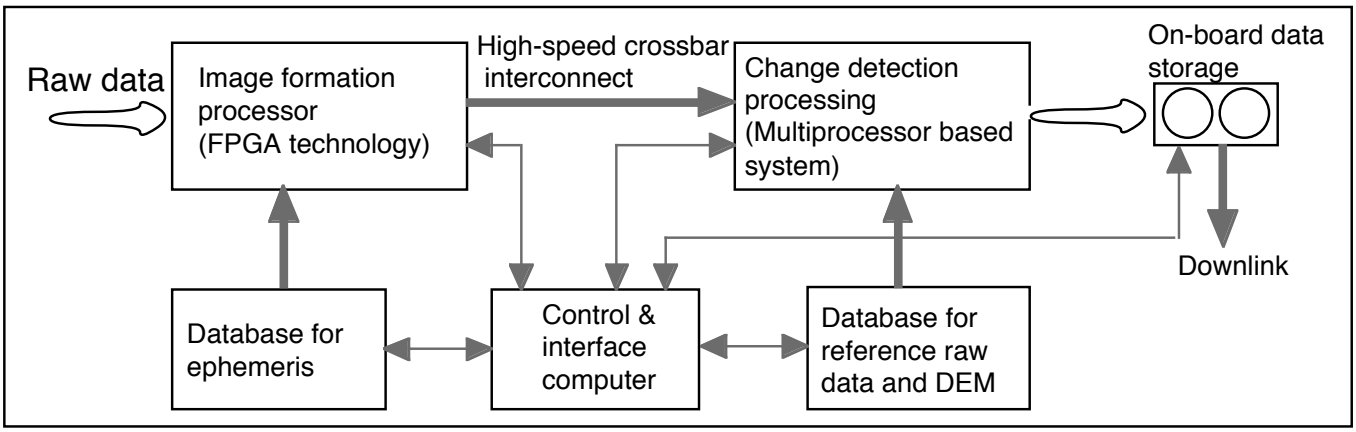

Figure 2. Functional block diagram of the hardware architecture of the CDOP.

The preliminary functional board layout of the hardware architecture is shown in Figure 3. The advantages of this approach include:

1) Flexible architecture to provide upgrade path via extra slots in the VME chassis to host more data channels.
2) FPGAs can be upgraded to accommodate more processing throughput when faster and larger FPGAs become available.
3) Room to add an external memory card with high speed Rocket I/O interface to expand the capabilities of the post processor.
4) Utilizing the built-in Rocket I/O interface to provide fast (up to 3 Gbps), dedicated data paths between the FPGA cards and the post processor.
5) Utilizing standard interface and COTS hardware to minimize cost and development time.

Fibre channel interface was chosen to input raw data and output processed data for compatibility with an existing airborne SAR test-bed (AIRSAR) and future UAVSAR's digital systems and with high speed RAID disks.

IV. DEVELOPMENT PLAN

The development of the change detection on-board processor is a 3-year effort. In year 1 we will define the processor specifications, hardware architecture, interfaces, and begin developing the FPGA image formation processor and the interferometric post processor in parallel. In year 2 we will complete the processor fabrication and preliminary software development to demonstrate the functionality of the CDOP. In year 3 we will optimize the processor performance to generate change detection data products in near real-time.

ACKNOWLEDMENT

The work carried out in this paper was performed at Jet Propulsion Laboratory, California Institute of Technology under contract with the National Aeronautics and Space Administration (NASA). The authors wish to thank NASA's Earth Science Technology Office for funding this technology development through the Advanced Information System Technology program.

REFERENCES

[1] Massonnet, D., M. Rossi, C. Carmona, F. Adragna, G. Peltzer, K. Feigl, and T. Rabaute, The displacement field of the Landers earthquake mapped by radar interferometry, *Nature,* vol. 364, pp. 138-142, 1993.

[2] Zebker, H.A., P.A. Rosen, R.M. Goldstein, A. Gabriel, and C.L. Werner, On the derivation of coseismic displacement fields using differential radar interferometry: The Landers earthquake, *Journal of Geophysical Research,* vol. 99, pp. 19617-19634, 1994.

[3] Bürgmann, R., D. Schmidt, R.M. Nadeau, M. d'Alessio, E.J. Fielding, D. Manaker, T.V. McEvilly, and M.H. Murray, Earthquake potential along the northern Hayward fault, California, *Science,* v. 289, pp. 1178-1182, 2000.

[4] Saatchi, S.; Moghaddam, M., Estimation of crown and stem water content and biomass of boreal forest using polarimetric SAR imagery, *Geoscience and Remote Sensing, IEEE Transactions on*, Vol. 38, Issue 2, Part 1, pp. 697-709, 2000.

[5] Alsdorf, D.E., J.M. Melack, T. Dunne, L.A.K. Mertes, L.L. Hess, and L.C. Smith, Interferometric radar measurements of water level changes on the Amazon floodplain, *Nature,* vol. 404, pp. 174-177, 2000.

[6] Shi, J.C., Chen, K.S., Van Zyl, J.; Kim, Y.; Njoku, E.G., Estimate relative soil moisture change with multi-temporal L-band radar measurements, *IGARSS '02 Conference Proceedings*, Vol. 1, pp. 647-649, 2002.

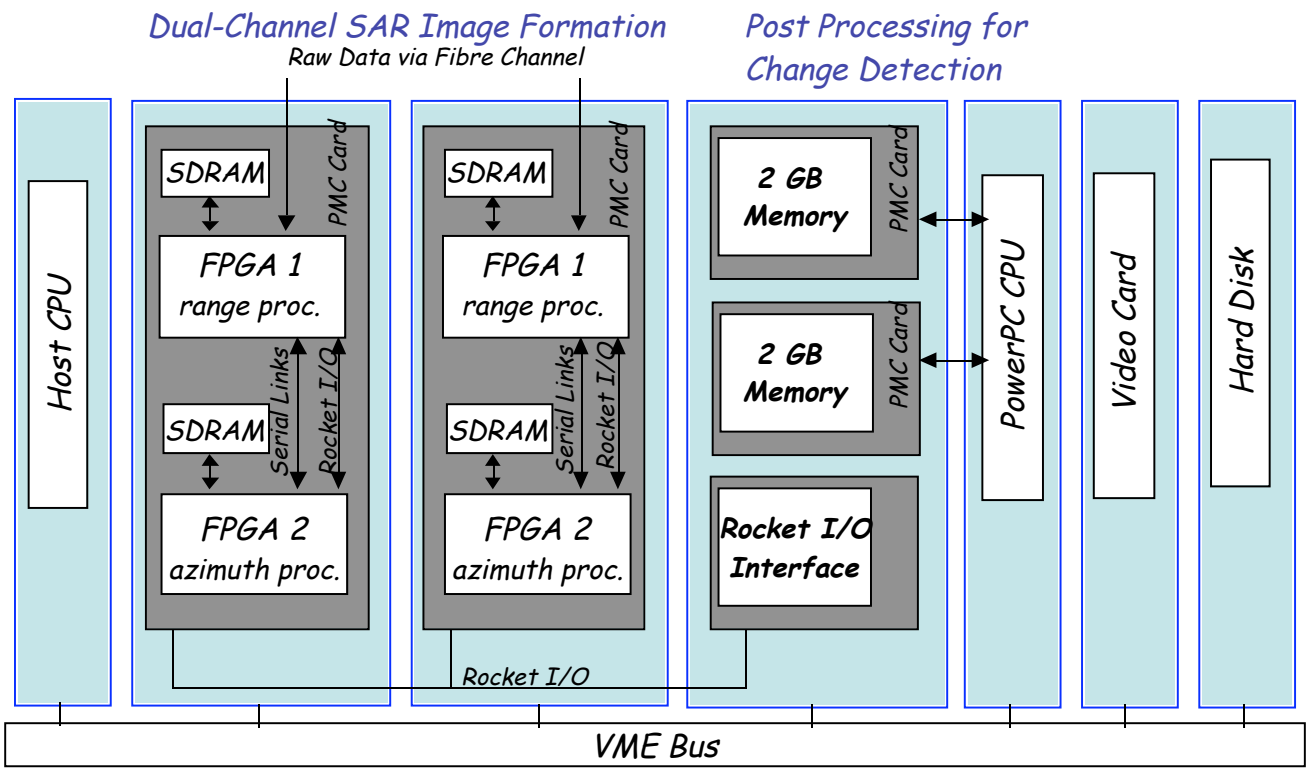

Figure 3. The VME-based hardware architecture of the CDOP.

Figure 3. Functional board layout of the VME-based CDOP.