ESTC 2003
College Park, MD, USA, 24-26 June 2003

Adaptive Data Analysis and Processing Technology (ADAPT) for Spacecraft

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Abstract *– The Adaptive Data Analysis and Processing Technology (ADAPT) project developed a prototype reconfigurable processor that used state of the art field programmable gate array technology. This project will develop and demonstrate algorithms and configuration programs to enable future missions by providing efficient development of on board processing and control systems that are reconfigurable in flight. This reconfigurable processing technology provides the flexibility of a general-purpose processor running software with the performance of a dedicated hardware processor.*

I. BACKGROUND

Many Earth Science Enterprise (ESE) science themes have identified instrument options and associated system requirements that require on board data processing and autonomous operations to reduce system development and operations cost while returning improved data and associated geophysical parameters required for future science needs. Adaptive computing is an essential element in fulfilling the requirements for on board data processing and autonomous operations required to meet the future mission needs. It enables efficient on board processing of instrument data that delivers information to scientists rather than raw data. It reduces the amount of data stored or transmitted to the ground and minimizes both the on board and ground data handling system requirements. Adaptive computing also enables highly autonomous instrument systems that can be reconfigured in-flight to optimize operations, and thus science return, during the mission lifetime. Improved data management and operations will reduce total mission cost for future ESE programs.

A. From Software and ASICs to FPGAs

In the past, general-purpose processors and custom hardware circuits have handled data processing onboard satellites. System flexibility was primarily associated with system software; ASICs could quickly execute a limited and fixed set of tasks where timing was critical.

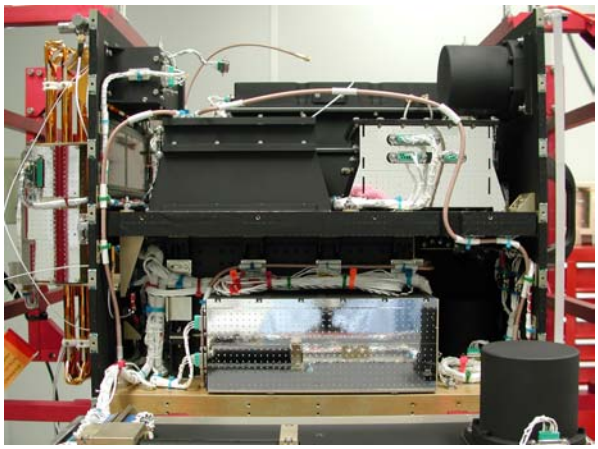
The field programmable gate array (FPGA), however, offers another option that combines execution speed approaching that of an ASIC, with the programmability of the general-purpose processor. SRAM-based FPGAs can rapidly reconfigure and have benefited from new developments in FPGA technology, which have produced larger and faster SRAM-based devices. Xilinx, a vendor of FPGA technology, produces the Virtex II device; the ADAPT hardware used these new FPGA devices in a reconfigurable module. ADAPT can function efficiently in a variety of space-based applications and therefore can provide the next step toward data processing and intelligent instrument control onboard satellites.

B. Adaptive Instrument Module (AIM)

ADAPT leveraged work performed at JHU/APL in development of the Adaptive Instrument Module (AIM) reconfigurable processor and the LaRC Reconfigurable Smart Module. The AIM is the first space borne reconfigurable processor, which launched on the Australian Fedsat 1 spacecraft on December 14, 2002. See Figure 1. JHU/APL designed and fabricated the AIM hardware; it used a prior generation Xilinx FPGA to perform reconfigurable processing. See Figure 2. FPGA configuration and readback verification is performed in software on the AIM, as opposed to hardware in the ADAPT.

C. Reconfigurable Data Systems Smart Module

The LaRC Reconfigurable Data Systems Smart Module is a multi-chip module that flies in the Gas and Aerosol Monitoring Sensorcraft (GAMS) system to generate the timing, clock, and control signals. LaRC designed and developed the hardware, FPGA design, and software. This module was developed as part of the GAMS Instrument Refinement Project funded by the ESE Instrument Incubator Program. This module also used prior generation FPGA technology.



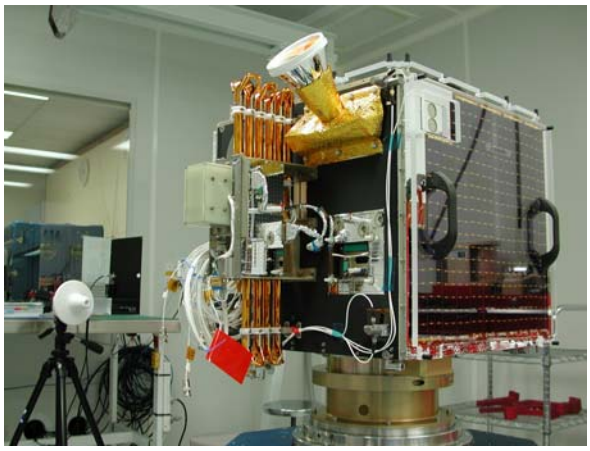


Fig. 1. The FedSat satellite during integration.

Fig. 2. The AIM module before integration into the FedSat satellite.

II. APPROACH

NASA LaRC and JHU/APL have collaborated to develop reconfigurable computing instruments for space-based instruments. LaRC has been responsible for the overall instrument design and the software; JHU/APL has been responsible for designing and developing the hardware.

ADAPT uses SRAM-based technologies and can reduce the amount of data stored or transmitted to the ground, which minimizes the data handling both on the satellite and on the ground. Adaptive computing can provide highly autonomous instruments that can be reconfigured in-flight to optimize both operations and science return. Improved data management and operations will reduce total cost of missions in future programs.

III. CURRENT STATUS AND PLANNED WORK

A. Current Status of Progress

1. The ADAPT board has been fabricated. See the photograph in Figure 3 and the block diagram in Figure 4.
2. The methodology for managing the Xilinx Virtex FPGAs has been tested and found functional. Three operations have been verified:
   - Read back of the Xilinx Virtex FPGAs,
   - Correction of upsets, such as SEUs, and
   - Flash programming of the configuration stream.
3. The Actel configuration manager design has been partially verified and programmed.
4. The Interface between configuration manager and PCI has been specified.
5. The PCI Interface Actel has been partially built and pieces have been simulated.
6. A CompactPCI host, chassis, power-supply and drives have been ordered and are to being configured.

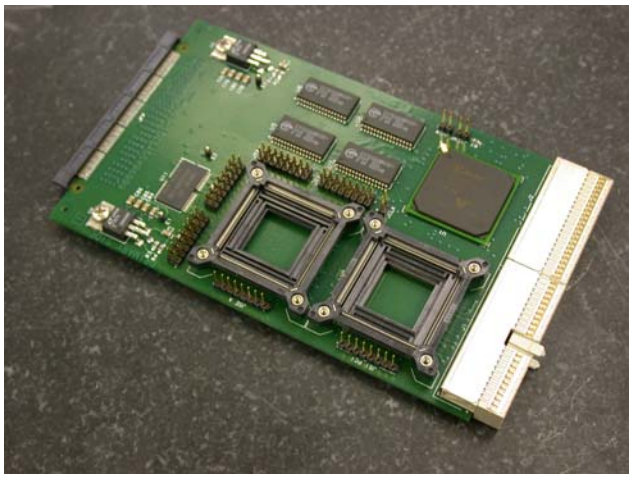


Fig. 3. The ADAPT board.

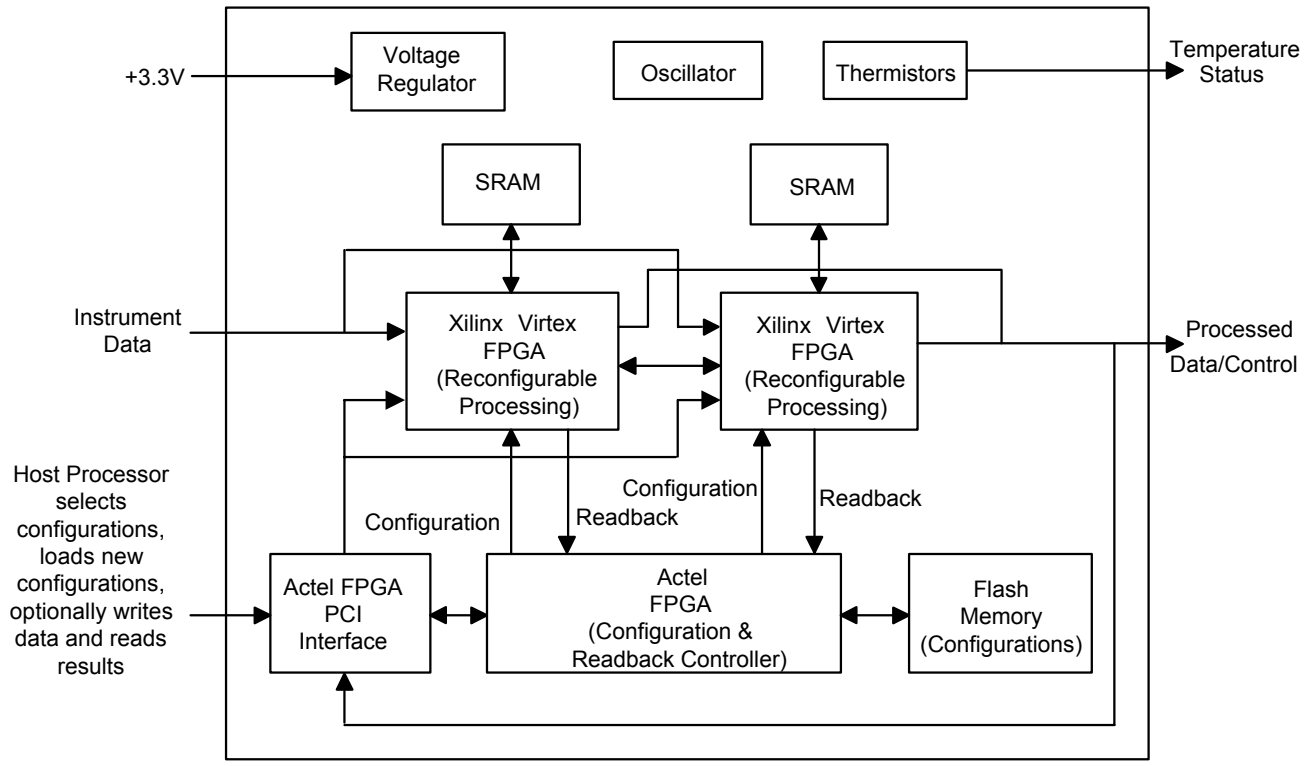


Fig. 4. Block diagram of the ADAPT board.

B. Planned Work

Final design and testing of the ADAPT PCI Actel will commence upon receipt of the needed equipment (CompactPCI Host / chassis). This will also greatly ease the testing of the configuration manager, which is not completed.

Software utilities need to be written to support flash programming and various ADAPT tasks. This will be mostly register bit-banging software based on the configuration manager protocol specification.

A flight version of the ADAPT hardware will be tested for radiation total dose and SEUs at the accelerator facility at Brookhaven National Laboratory. The radiation tests of ADAPT will prepare it for qualification for space flight. We expect the testing and report to take between 9 and 12 months.

IV. DISCUSSION – NOVELTY AND UTILITY

This improved performance along with the adaptability of this technology provides significant benefits at several levels:

1. Engineering setup times for science observations will be greatly reduced. The entire sensor data processing can be expressed in a configuration file that loads into the FPGA. Mission operations merely have to specify which configuration file is to be loaded into the FPGA. The loading process takes on the order of 1 second. The ADAPT card will be able to store at least 20 FPGA configurations.

2. The FPGAs offer extremely dense performance in terms of processing per chip. SRAM-configured FPGAs offer far higher performance over the current state of the art in space electronics. Furthermore, this performance permits several levels of fault tolerance: 1) if a device only has a partial failure, a new configuration can map around the cells that have failed, 2) two FPGA chips can easily fit on a 3U CompactPCI card. The second FPGA can take over if the first FPGA totally fails.

3. Although the basic physical hardware design remains unchanged, the hardware for the control and data interfaces can easily be programmed for a specific instrument and/or spacecraft data system architecture. One of 17 different I/O standards can be selected for each FPGA I/O pin. This allows flight qualification of the basic hardware independent of the detailed hardware design for a specific system. This minimizes

the cost of developing the basic hardware for each instrument and allows the physical design to be easily reprogrammed for any system architecture. Loading a different configuration file programs the FPGA.

4. This approach also minimizes overall instrument or system development time by allowing physical and electrical testing of the hardware to proceed concurrently with the detailed design and programming of the FPGAs. Also, if an error in the design is detected during system level testing, the hardware can be easily reconfigured without having to physically remove the processor from the system. This minimizes the impact on the project schedule and risk to the flight hardware.

5. The use of SRAM-based FPGA technology enables the hardware design to be reconfigured in flight to overcome both hardware and software errors that may be detected after launch during mission operations. This reduces overall mission risk which is becoming more important as flight system development times and budgets decrease in the current faster, cheaper, and better environment.

The ability to reconfigure the ADAPT board in flight allows the processor functions to adapt to changing mission conditions and also allows improved onboard processing algorithms to be uploaded to the instrument. The reconfigured processor can optimize mission operations to exploit science "targets of opportunity" as the mission progresses and also take advantage of improved data processing algorithms to return the most science for the minimum cost. At least 20 configurations can be stored on the card, and new configurations can be loaded at any time.

V. TECHNICAL CHALLENGES

There are three technology challenges to be overcome. The first is that the configuration SRAM in the Xilinx FPGAs is susceptible to SEU. These upsets can result in improper device operation. Fortunately, the contents of the configuration SRAM can be read out and compared to what was originally loaded in. The first generation AIM reconfigurable processor developed at JHU/APL checks the configuration SRAM with the aid of a microcontroller. If an error were discovered, the Xilinx FPGA in the AIM would be reloaded with the correct configuration. ADAPT will use an Actel FPGA based state machine to read out the configuration memory and compare it to the expected data. It is expected that the Xilinx FPGA configuration SRAM can be checked every few seconds. This greatly limits the improper data that might be produced.

The second technology challenge is packaging. The highest capacity radiation-hard Xilinx FPGAs are only available in a 560-pin ceramic grid column array package. The best fabrication process for using this package, in terms of mechanical durability and thermal characteristics, needs to be identified. As a fallback, a lower capacity Xilinx FPGA in a quad flat pack package can be used instead of the ceramic grid column array package.

The third technology challenge is innovation in developing algorithms for cellular automatons for self-healing. These are on the frontiers of research and unproven. The fallback is that read-back verification can provide a stable baseline of operation and functionality should the cellular automatons prove unreliable.

VI. CONCLUSION

We expect to complete the architecture and algorithms for ADAPT within a year, and, at the end of the second phase of development, flight hardware. The track record of NASA LaRC and JHU/APL working on similar projects, such as AIM, indicates a measure of confidence that ADAPT will be successful. AIM successfully launched on the Australian FEDSAT satellite on December 14, 2002 and is currently operating in space.

REFERENCES

[1] "Adaptive Instrument Module - A Reconfigurable Processor for Spacecraft Applications," R. F. Conde, A. Garrison Darrin, F. C. Luers, S. Jurczyk, N. Bergmann and A. Dawood. Military and Aerospace Programmable Logic Devices Conference 1999.

[2] http://www.crcss.csiro.au

[3] http://www.itr.unisa.edu.au/crcss/FedsatLaunch.htm