GeoSTAR-II Technology Risk Reduction for the NASA Decadal Survey PATH Mission

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Abstract— The NRC Decadal Survey, identifying the continuous sounding of atmospheric temperature and humidity as an important science goal, selected the PATH (Precipitation and All-weather Temperature and Humidity) mission for further development. The PATH platform located in geostationary orbit, will utilize STAR technology to image a large portion of the earth simultaneously with 25 km resolution and no moving parts. NASA selected the GeoSTAR-II to demonstrate key technologies which are required for the PATH mission. We describe developments of these key technologies which include low power digitizers, low power high speed correlators, low noise amplifiers, compact downconverters and compact array technologies.

Index Terms — millimeter-wave amplifiers, high speed digitizer, low power digital ASIC, microwave interferometry, microwave remote sensing.

1. INTRODUCTION

Measurements of atmospheric temperature and humidity profiles are of great importance to atmospheric science and weather forecasting. Indeed, the assimilation of microwave satellite data into weather forecasting models has had a large effect on the accuracy of weather forecasting[1] and climate modeling. Recognizing the importance of this data product, the National Research Council (NRC) Decadal Survey selected the Precipitation All-weather Temperature and Humidity (PATH) mission for further study.

The PATH mission would provide near continuous coverage of temperature and humidity profiles over a large portion of the globe. Operating at microwave and millimeter-wave frequencies, PATH can penetrate clouds provide soundings into the lower troposphere. Continuous coverage is only possible from geostationary orbit which creates the requirement of a large effective aperture to obtain a spatial resolution of 25 km, the footprint needed by the weather forecasting and climate modeling community.

The preferred approach towards this goal is a Synthetic Thinned Aperture Radiometer (STAR), in which the thermal image is formed interferometrically. This provides for a large effective aperture without a large antenna, while imaging the entire field of view with no moving parts. This approach has been demonstrated by ESA's SMOS mission [2] (for soil moisture and ocean salinity measurements) from low Earth orbit, but at much lower frequencies than those required by PATH. The temperature and humidity sounding requirements of PATH require operation with a minimum band suite covering 50-60 GHz and 165-183 GHz. The GeoSTAR prototype [3] demonstrated that such an instrument operating at millimeter wavelengths could be calibrated The combination of operating frequency, sensitivity, field of view and angular resolution all create requirements for low noise receivers in large numbers, low power digitizers, large low power cross correlators and compact receiver array technologies. The GeoSTAR-II program has made significant progress in each of these areas leading to large scale engineering demonstrations of a PATH type system.

2. PATH OBSERVING REQUIREMENTS

The current suite of low-Earth orbiting (LEO) microwave sounders provide global retrievals of key atmospheric parameters approximately every six hours. Even with the addition of planned LEO instruments, coverage will not improve to below several hours. The PATH mission seeks to improve upon this regionally. The decadal survey created notional requirements for such a mission which have been refined to provide a basis for mission trade-studies. These requirements are shown in Table 1. These requirements are largely derived from the AMSU A and B on-orbit performance, but with 15 minute refresh rates over a 5000 km field of view and should not be viewed as the PATH mission requirements, but rather those which might push the technology requirements upon flowdown.

The requirements in Table 1 have been used to perform mission studies as well as design and technology trades. One such study identified key technology areas which would require additional investment prior to a PATH mission was ready for development.

Table 1. PATH Notional Requirements (Refined)

Frequency (GHz)	Hor. Res (km)	Res BW (MHz)	Refresh Rate (min)	Accuracy (K)
50.3	50	300	15	0.3
52.8	50	300	15	0.3
55.5	50	300	15	0.3
57.29	50	300	15	0.3
183.31	25	1000	15	0.4
180.31	25	1000	15	0.4
176.31	25	1000	15	0.4
165	25	1000	15	0.4

These driving requirements, shown in Table 2 became the basis of a technology development program to advance the readiness of a future mission. These areas include low power high speed digitizers, low-power large cross correlators, mass production of low noise 165-183 GHz receiver front ends, demonstration of scalable sub-array modules which include beam forming structures, analog signal processing and distribution, reference oscillator distribution and low power efficient DC-DC supplies. Under the GeoSTAR-II program significant advances have occurred in several of these areas since the release of the decadal survey. These advances are described below.

Table 2. PATH Driving Technologies and Performance Metrics

		Goal	CBE
Correlator	Power	250 uW/corr	224 uW/corr*
	BW	500 MHz	375 MHz
Module	Gain	15 dB	~10 dB
Boards	BW	165-183 GHz	165-183 GHz
	Noise	400 K (3.7 dB)	~500K (4.3 dB)
	Power	42mW	60 mW
Sub-Array	Mass	2kg	3.5 kg
Module	Mech Tol	0.001”	tbd
IF	Mass	20 kg	~15 kg
Subsystem	BW	>500 MHz	>1 GHz
	Gain	>40 dB	>40 dB
	Power	0.94 mW/dB	0.69 mW/dB

2. High Speed Digital ASICs

A. Large N Digital Cross Correlator

The GeoSTAR demonstrator had 24 receiver elements, eight per arm in each of three arms. The correlator must multiply all signals from each arm against the other 2. This required a total of 128x4 total products, each with one bit resolution. With a bandwidth of 64 MHz , this was easily achieved using standard FPGA chips. The PATH requirements of Table 1 lead to a STAR system which has ~128 elements per arm, operating with a bandwidth of 500 MHz and a resolution of 2 bits, the 128^2 x 4 products would easily exceed the capacity of a large FPGA. Furthermore, if one attempted to employ an array of FPGAs to carry out the task, the power budget would exceed 500 W!

It was recognized that low power CMOS technology could employed to efficiently perform this function. As a technology demonstration, we developed a 17x17 correlator chip operating with 500 MHz bandwidth using 90 nm CMOS technology. The GeoSTAR-II ASIC correlator chip is designed to accept 2 bit inputs at 1000 MHz clock rate through standard LVDS lines. The correlator core was designed to be scalable and requires 250 μW per correlation, which would result in a core power dissipation of 50W for the 128 element per arm 183 GHz PATH correlator. At this power level, the correlator is no longer considered a driving requirement.

The correlator chip was designed as a correlate-accumulate logic circuit. In addition to cross correlation, the chip also provides totalizers, which capture the total power in each of the inputs. The totalizer outputs can be used to level set the signals from the receivers. In a automatic gain control loop. The chip is designed to dump the accumulator output for further to a small FPGA for longer integration periods. Nanosim [4] simulations performed on the ASIC confirm all design goals, with the exception of chip speed, which is limited to 750 MHz sample rate. This was a design related problem and not a technology limit.

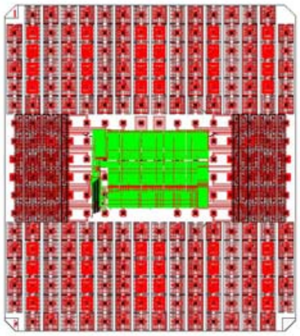

Figure 1. Physical layout of ASIC correlator chip. The 17x17 input chip was processed on 90 nm CMOS. The chip size is 1mm x 1.2 mm and the green area in the center is the logic core. The red pads on the perimeter are primarily the LVDS inputs.

The chip has been processed on the IBM 90 nm low power CMOS process [5] through the TAPO [6]. The chips have been packaged and are currently undergoing testing with an HP82000 IC tester. Full testing requires high speed customized test circuits which are being developed.

B. Low-power high speed 2-bit Analog to Digital Converter

While the baseline design for GeoSTAR-II utilizes a commercial 8-bit A/D converter (truncated to two bits), the part draws more than 1W. At that power level, the A/D converter would be a large system driver for the PATH mission. It was recognized that the same process used for the correlator was ideal for the development of a 2-bit 1 GSPS A/D converter.

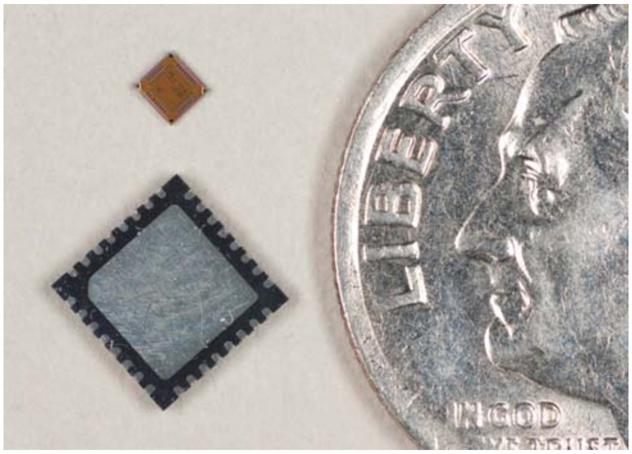

Figure 2. 2-Bit Analog to Digital Converter. This high speed chip also processed on 90 nm CMOS will operate faster than 1 GSPS while drawing only 32.5 mW

The A/D has 6-bit programmable offset bit levels and LVDS outputs for testing and integration with the correlator. The logic core of the chip consumes 2.5 mW of power and the entire chip draws 32.5 mW. This order of magnitude improvement in performance removes the A/D power as a design consideration for the PATH system. The process compatibility with the correlator ASIC allows for future integration on the final chip, eliminating the need for LVDS input/output drivers, saving substantial power. A photograph of the A/D chips is shown in Figure 2. These chips are also awaiting testing.

3. COMPACT 183 GHZ DOWNCONVERTERS

A low noise surface mount downconverter operating at 183 GHz has already been demonstrated [7]. The expected performance is below 400K at room temperature, enabling the 0.4K PATH performance specification with the GeoSTAR-II design. The large number of receivers required for PATH requires that the modules must be easily assembled and have repeatable performance. For the GeoSTAR-II effort, 50 modules will be manufactured.

Each module comprises three InP chips, two amplifiers and an I/Q downconverter. The amplifiers have all been tested using on-wafer probing techniques, allowing chip selection prior to module assembly and increasing the module yield. Only a few of the modules have been assembled to date and the testing program is underway.

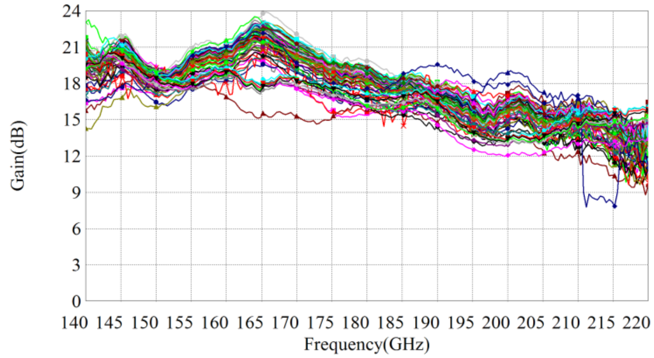

Figure 3. Wafer probe data of the ensemble gain of a large number of 140-210 GHz low noise amplifiers.

4. SUB-ARRAY MODULE

The GeoSTAR instrument with only 24 receivers, utilized single unit building blocks. Recognizing PATH as a goal, GeoSTAR-II required a different approach. With 128 receivers per arm and feed horns antennas only a few wavelengths in diameter, integrating multiple receivers in a single “tile” which can be replicated to fill out the array became in important design consideration, particularly for instrument integration and test.

The 183 GHz concept is shown in Figure 4. The sub-array module comprises beam forming feed horns, a local oscillator distribution manifold, IF and bias distribution circuit boards, a local oscillator multiplier and a lightweight structural support framework.

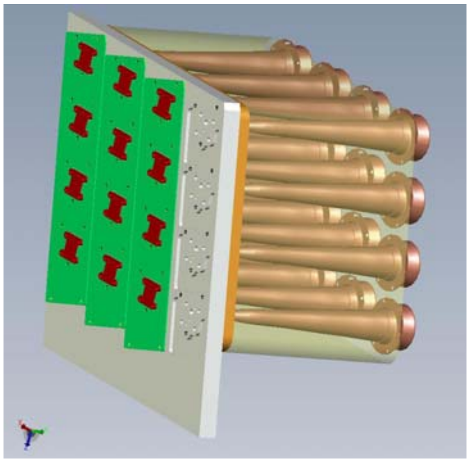

Figure 4. Sub-array tile concept. The feed horns on the right are mounted to the LO manifold plate. On the other side of the manifold, the receiver modules (red)are connected to the plate and make all low frequency electrical connections through the circuit board (green)

The feed horns are manufactured in electroformed copper with a minimum wall thickness of 375μm to minimize mass. The local oscillator manifold forms the backbone of the tile, serving as the primary mechanical interface. The primary function of the manifold is to distribute the 87-92 GHz local oscillator signal. A single waveguide input is divided 16 ways to each of the modules. The basic division network is based upon a design developed for the Atacama Large Millimeter Array (ALMA)[8], and is manufactured in a split block of machined aluminum.

The receiver modules are mechanically mounted to the waveguide manifold block, but they are soldered to the IF/bias boards. Each board provides ~35 dB of IF gain and programmable bias to the modules. Signals are passed from the boards to the correlator subsystem via lightweight coaxial cables. The entire sub-array module has a mass of 3.5 kg or 84 kg for the full complement of PATH 183 GHz receivers..

5. Conclusion

A geostationary microwave sounder has been recommended by the NRC Decadal Survey for Earth Science. Initial demonstrations of the interferometric techniques recommended have been shown to yield reliable brightness temperature data. A risk reduction activity to fully realize technologies necessary to meet the mission requirements in a cost-effective manner has been funded by NASA. Significant progress has been made in four technology areas; digital correlators, high speed A/D chips, compact downconverters and integrated sub-array modules.

Acknowledgements

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